Homework Assignment 3

(Due 4th October 2013 at the beginning of the class)

(1) Given the function $f = x_1x_2x_4 + x_1x_3\bar{x}_4 + \bar{x}_1\bar{x}_2\bar{x}_3$, a straightforward implementation in an FPGA with three-input LUTs requires four LUTs. Show how it can be done using only 3 three-input LUTs. Label the output of each LUT with an expression representing the logic function that it implements. [5]

(2) Implement the following function using three 2-input LUTs [5]

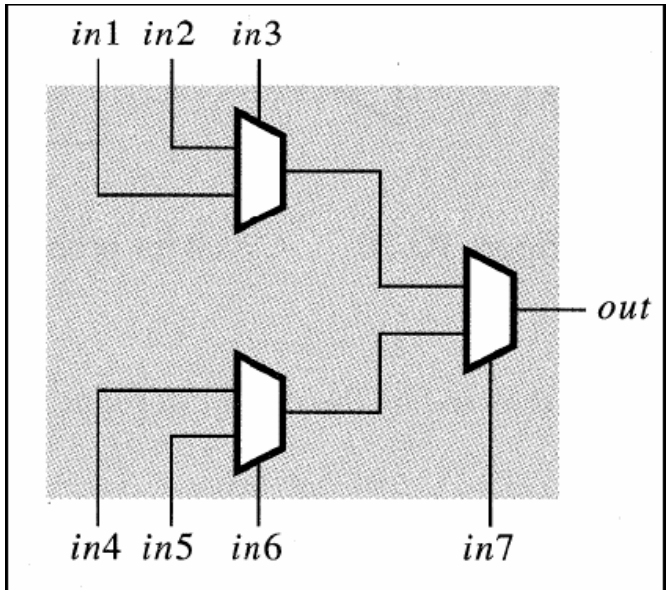
$$F = AB\overline{C} + \overline{A}C\overline{D} + ABD + \overline{B}C\overline{D}$$

(3) What is the difference between a Hard Macro and a Soft Macro [2]

(4) Illustrate how to implement the following equations in an eight-to-one mux [3]

$$F = A\overline{B} + B\overline{C} + C\overline{D}$$

(5) Assume that a gate array contains the type of logic cell depicted in the figure below. The inputs in1, …, in7 can be connected to either 1 or 0, or to any logic signal. [5]



Show how the logic cell can be used to realize $f = X_1 \cdot X_2 + X_3$
Show how the logic cell can be used to realize $f = X_1 \cdot X_3 + X_2 \cdot X_3$

(6) Assume that a gate array exists in which the logic cell used is a three-input NAND gate. The inputs to each NAND gate can be connected to either 1 or 0, or any logic signal. Show how the following logic functions can be implemented in the gate array. [5]

$$f = x_1 x_2 + x_3$$
$$g = x_1 x_3 x_4 + x_2 x_3 \overline{x_4} + \overline{x_1}$$

(7) Illustrate how to implement the following functions using a four-to-one multiplexer. You can use 1, 0, the true and complement of each signal as inputs and select lines to the multiplexer: [5]

$$F = A \oplus B \oplus C$$
$$G = A + \overline{B}C$$