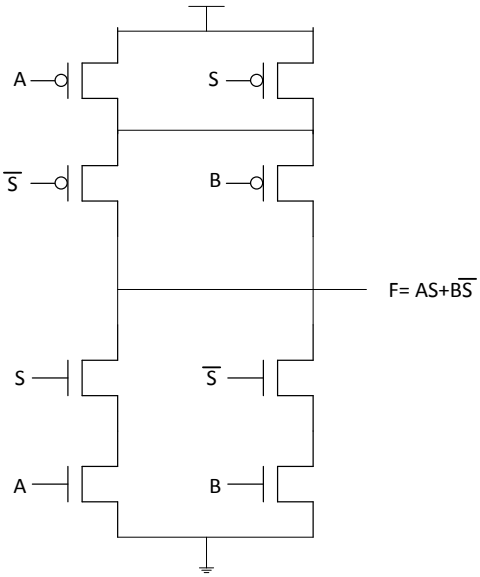
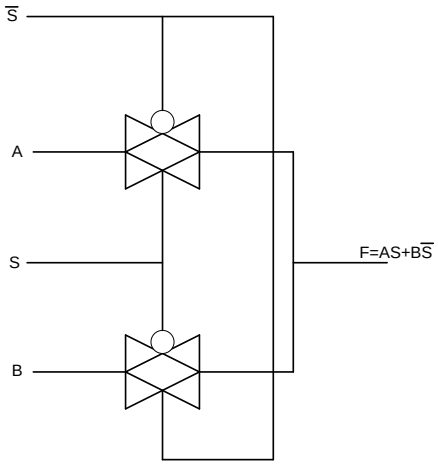
Solutions to HW1

(1) NOR structure is preferred for pseudo-NMOS, as it completely avoids series transistors. NAND structure is preferred in static CMOS, as there is no series stack of PMOS transistors.

(2)



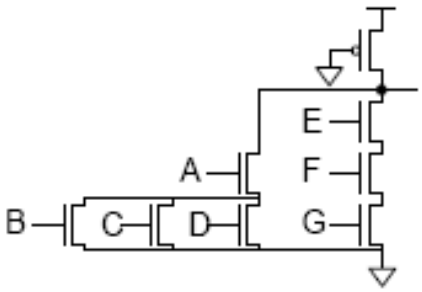


(3) Degraded buffer.

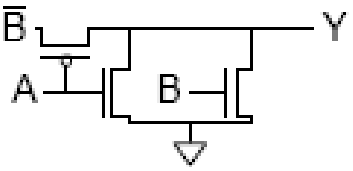
When $V_{in}= V_{DD}$, then $V_{out}=V_{DD}-V_{TN}$

When $V_{in}= 0$, then $V_{out}=|V_{TP}|$

(4)



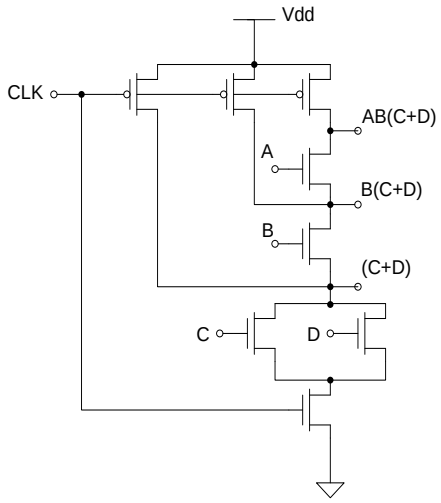
(5)



(6) A= $V_{dd} - V_T$, B= $V_{dd} - V_T$, C= $V_{dd} - 2V_T$

The last transistor won't be on because it's a PMOS and gate voltage (V_{dd}-V_T) is higher than source voltage (V_{dd}-$2V_T$).

(7)



(8) All the PMOS transistors will have size of 6W and the NMOS transistors will be of W.