EE434 ASIC & DIGITAL SYSTEMS
MIDTERM EXAM 2
10th November 2008

School of Electrical Engineering and Computer Science
Washington State University
Maximum Points: 25
Time: 2.10 pm-3 pm

Problem 1:
(a) Do you see any problem with the following verilog code? Please explain [3]

```
always @ (posedge clk, posedge reset)
        If (reset) q <= 0;
                else q <= d;

always @ (set)
        If (set) q <= 1;
endmodule
```

(b) When we tried to simulate the following code, sometimes we observed ‘x’ at the output. What is the reason behind such observation? Explain. [2]

```
module mux_2 (input [3:0]  d0, d1,
              input   s,
              output [3:0]   y);

tristate t0 (d0, s, y);
tristate t1 (d1, s, y);
endmodule
```

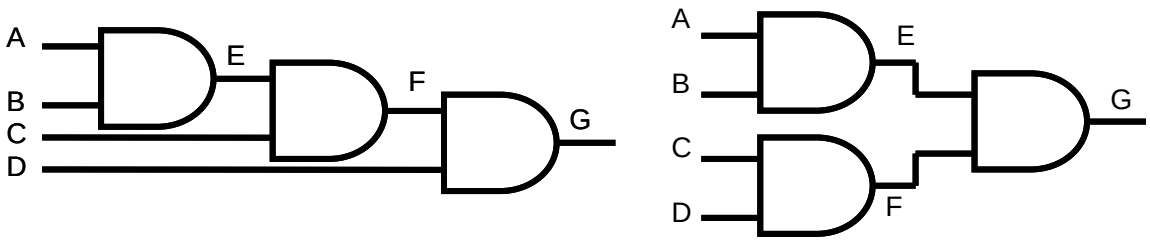
Problem 2:
(a) Following is the module declaration of a D flip-flop with an ***asynchronous active-low reset.*** Complete the description of the flip-flop using verilog. [3]

Module flipflop (D, Clock, Resetn, Q);
Input D, Clock, Resetn;
Output Q; reg Q;

Always @ (…….)
……
……..

endmodule

(b) Among the following two circuits which one is more susceptible to glitching noise and why? Assume all the gates to have same delay. [3]



(a) (b)

(c) The following piece of verilog code is to be used to model a Mux. When synthesized would it behave like a Mux? If not then what it would be? Explain [3]

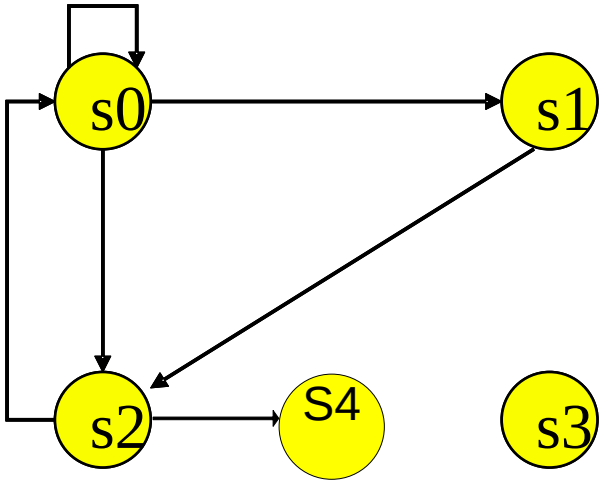
```
module mux (input   [3: 0]   d_0, d_1,
                             input s,
                             output reg [3: 0] y);

always @ (posedge s)
        if (s) y <= d_1;
        else y <= d_0;
endmodule
```

Problem 3:

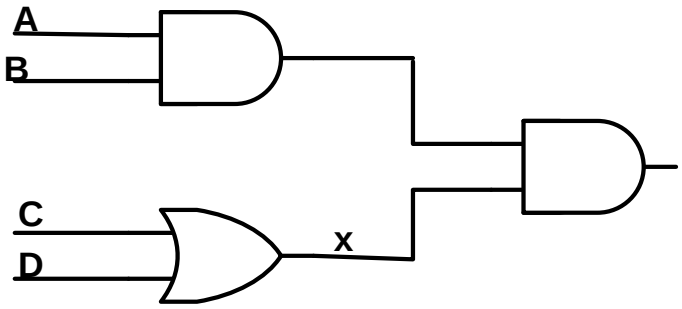
(a) What is "homing sequence" for any state machine? Can we consider the global reset signal as a homing sequence? Why? [2]

(b) What are the problems in the following state machine? How can you rectify those? [2]



Problem 4:

(a) What will be the input test vector to test stuck-at-1 fault at the node x in the following circuit? [3]



(b) Show that in the exclusive-OR circuit of the following figure faults c s-a-1 and f s-a-1 are equivalent [4]