

Homework Assignment 2 (Due Oct. 2, 4:15pm)

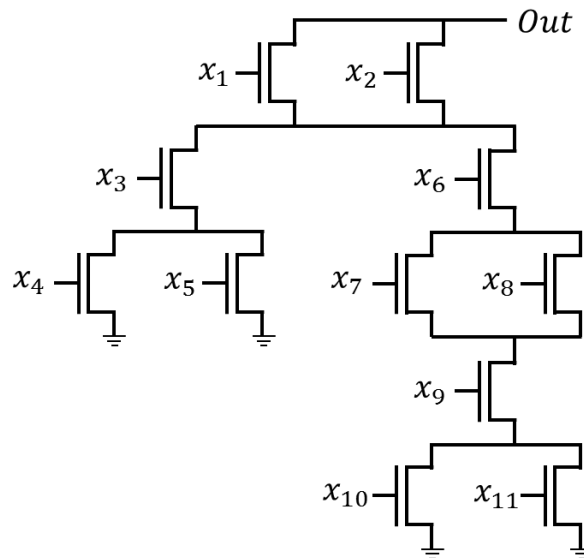
- (1) **[Static CMOS, 10 points]** Draw a transistor-level schematic for the following Boolean function (Available input: A, B, C, D, E, F, G). # TRs should be less than 20.

$$Y = A \cdot B + C \cdot (D \cdot E \cdot (F + G))$$

- (2) **[Static CMOS, 10 points]** Draw a transistor-level schematic for the following Boolean function (Available input: A, B, C, D, \bar{A} , \bar{B} , \bar{C} , \bar{D}). # TRs should be less than 24.

$$Y = A \oplus (B + \overline{C \oplus D})$$

- (3) **[Transistor sizing, 10 points]** The following shows a schematic of an NFET network of a static CMOS gate. Size the transistors. Timing constraint: $\tau = R_n C_L$ where R_n is the resistance of a 1X NFET and C_L is a load cap. The total width should be less than 55X.



(4) **[Design and transistor sizing, 20 points]** Draw a PFET network for the static CMOS gate shown above (in Problem 3). Use only 11 PFETs. Size the transistors. Timing constraint: $\tau = R_n C_L$ where R_n is the resistance of a 1X NFET and C_L is a load cap. $\mu_n = 3\mu_p$. The total width should be less than 120X.