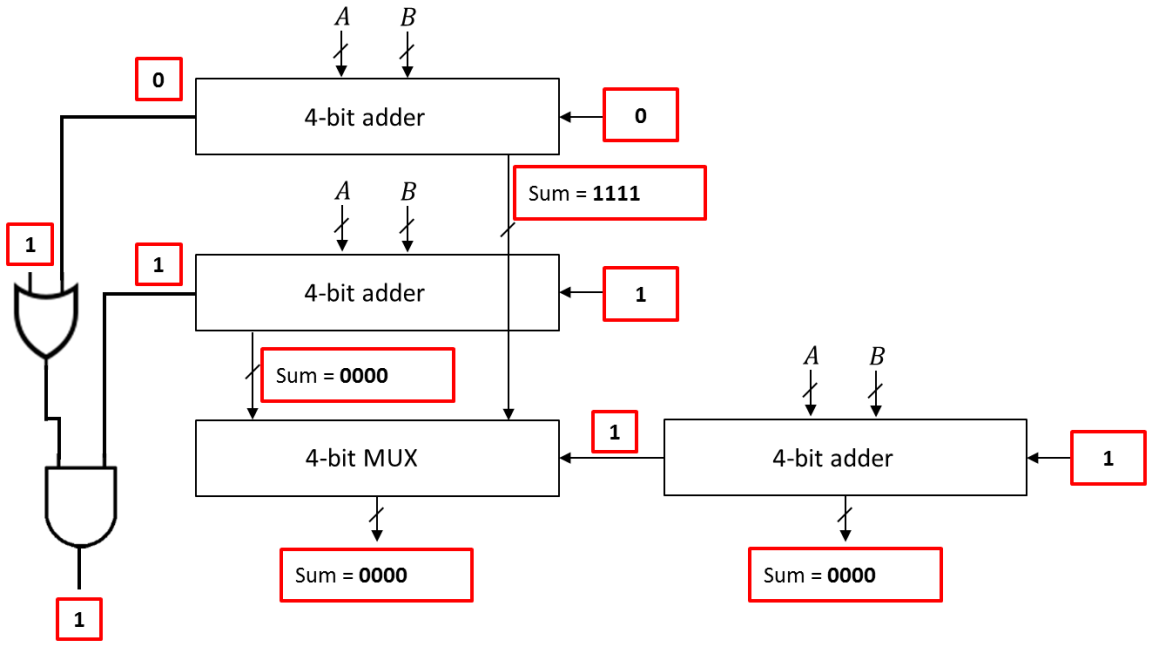
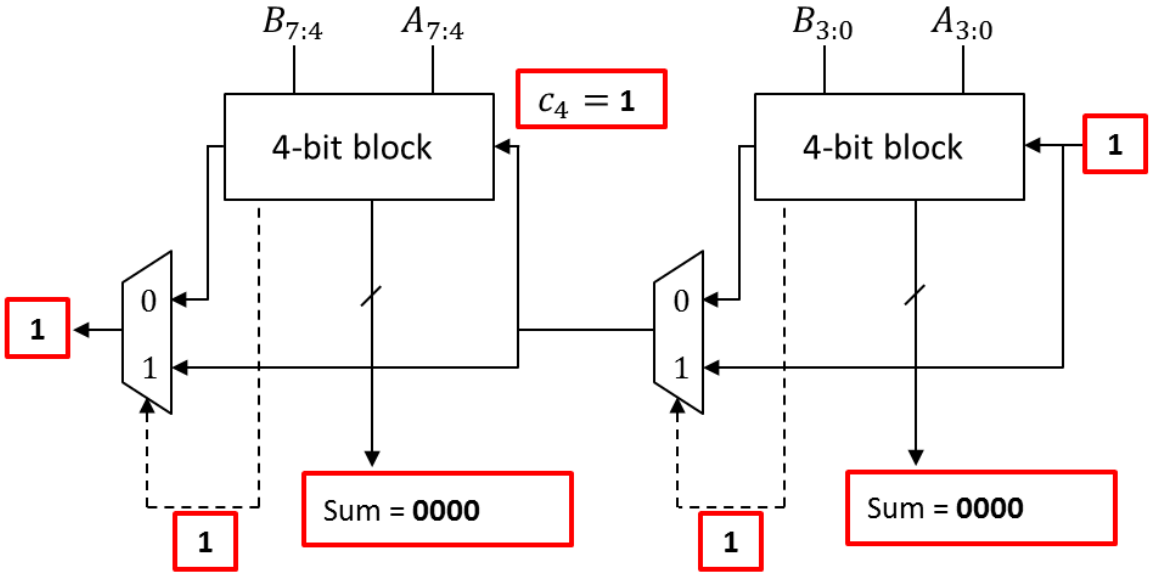
Homework Assignment 4
(Due Dec. 9, 11:59pm)

(1) **[Adder, 10 points]** Add the following three numbers using the carry select adder shown below. A=10101010, B=01010101, Cin=1 (Fill in the blank boxes).



(2) **[Adder, 10 points]** Add the following three numbers using the carry skip adder shown below. A=10101010, B=01010101, Cin=1 (Fill in the blank boxes).



(3) **[Adder, 10 points]** Add the following three numbers using the conditional sum adder shown below. A=11101110, B=01111001, Cin=1 (Fill in the blank boxes).

	i:	7	6	5	4	3	2	1	0	
	A_i:	1	1	1	0	1	1	1	0	
	B_i:	0	1	1	1	1	0	0	1	
Step 1	S_i^0:	1	0	0	1	0	1	1		$CI_0 = 1$
	CO_i^0:	0	1	1	0	1	0	0		
	S_i^1:	0	1	1	0	1	0	0	0	
	CO_i^1:	1	1	1	1	1	1	1	1	
Step 2	S_i^0:	0	0	0	1	0	1			
	CO_i^0:	1		1		1				
	S_i^1:	0	1	1	0	1	0	0	0	
	CO_i^1:	1		1		1		1		
Step 3	S_i^0:	0	1	0	1					
	CO_i^0:	1								
	S_i^1:	0	1	1	0	1	0	0	0	
	CO_i^1:	1				1				
Result	1	0	1	1	0	1	0	0	0	

(4) **[Adder, 20 points]** The delay of an AND (OR) gate is Δ and the delay of a two-level (sum-of-product) logic is 2Δ. We are designing a 1024-bit Kogge-Stone adder. Represent c_{87} hierarchically using group-generated and group-propagated carries $(g_{i:k}, p_{i:k})$ and c_0 (primary carry-in), then calculate the delay to obtain c_{87} assuming all the primary input signals are available at time 0.

$$c_{87} = g_{86:0} + p_{86:0} \cdot c_0$$

$$g_{86:0} = g_{86:23} + p_{86:23} \cdot g_{22:0}, \quad p_{86:0} = p_{86:23} \cdot p_{22:0}$$

$$g_{86:23} = g_{86:55} + p_{86:55} \cdot g_{54:23}, \quad p_{86:23} = p_{86:55} \cdot p_{54:23}$$

$$g_{86:55} = g_{86:71} + p_{86:71} \cdot g_{70:55}, \quad p_{86:55} = p_{86:71} \cdot p_{70:55}$$

$$g_{86:71} = g_{86:79} + p_{86:79} \cdot g_{78:71}, \quad p_{86:71} = p_{86:79} \cdot p_{78:71}$$

$$g_{86:79} = g_{86:83} + p_{86:83} \cdot g_{82:79}, \quad p_{86:79} = p_{86:83} \cdot p_{82:79}$$

$$g_{86:83} = g_{86:85} + p_{86:85} \cdot g_{84:83}, \quad p_{86:83} = p_{86:85} \cdot p_{84:83}$$

$$g_{86:85} = g_{86} + p_{86} \cdot g_{85}, \quad p_{86:85} = p_{86} \cdot p_{85}$$

Delay = 2Δ (to generate $g_i(\Delta)$ and $p_i(2\Delta)$) + 2Δ (for $g_{i:i-1}$) + 2Δ (for $g_{i:i-3}$) + 2Δ (for $g_{i:i-7}$) + 2Δ (for $g_{i:i-15}$) + 2Δ (for $g_{i:i-31}$) + 2Δ (for $g_{i:i-63}$) + 2Δ (for $g_{86:0}$) + 2Δ (for c_{87}) = 18Δ

(5) **[Adder, 20 points]** The delay of an AND (OR) gate is Δ and the delay of a two-level (sum-of-product) logic is 2Δ. We are designing a 1024-bit carry-lookahead adder. Represent c_{87} hierarchically using group-generated and group-propagated carries $(g_{i:k}, p_{i:k})$ and c_0 (primary carry-in), then calculate the delay to obtain c_{87} assuming all the primary input signals are available at time 0.

$$c_{87} = g_{86} + p_{86} \cdot g_{85} + p_{86} \cdot p_{85} \cdot g_{84} + p_{86} \cdot p_{85} \cdot p_{84} \cdot c_{84}$$

$$c_{84} = g_{83:80} + p_{83:80} \cdot c_{80}$$

$$c_{80} = g_{79:64} + p_{79:64} \cdot c_{64}$$

$$c_{64} = g_{63:0} + p_{64:0} \cdot c_0$$

$$g_{63:0} = g_{63:48} + p_{63:48} \cdot g_{47:32} + p_{63:48} \cdot p_{47:32} \cdot g_{31:16} + p_{63:48} \cdot p_{47:32} \cdot p_{31:16} \cdot g_{15:0}$$

$$p_{63:0} = p_{63:48} \cdot p_{47:32} \cdot p_{31:16} \cdot p_{15:0}$$

$$g_{63:48} = g_{63:60} + p_{63:60} \cdot g_{59:56} + p_{63:60} \cdot p_{59:56} \cdot g_{55:52} + p_{63:60} \cdot p_{59:56} \cdot p_{55:52} \cdot g_{51:48}$$

$$p_{63:48} = p_{63:60} \cdot p_{59:56} \cdot p_{55:52} \cdot p_{51:48}$$

$$g_{63:60} = g_{63} + p_{63} \cdot g_{62} + p_{63} \cdot p_{62} \cdot g_{61} + p_{63} \cdot p_{62} \cdot p_{61} \cdot g_{60}$$

$$p_{63:60} = p_{63} \cdot p_{62} \cdot p_{61} \cdot p_{60}$$

Delay = 2Δ (for p_i) + 2Δ (for $g_{i:i-3}$) + 2Δ (for $g_{i:i-15}$) + 2Δ (for $g_{i:i-63}$) + 2Δ (for c_{64}) + 2Δ (for c_{80}) + 2Δ (for c_{84}) + 2Δ (for c_{87}) = 16Δ