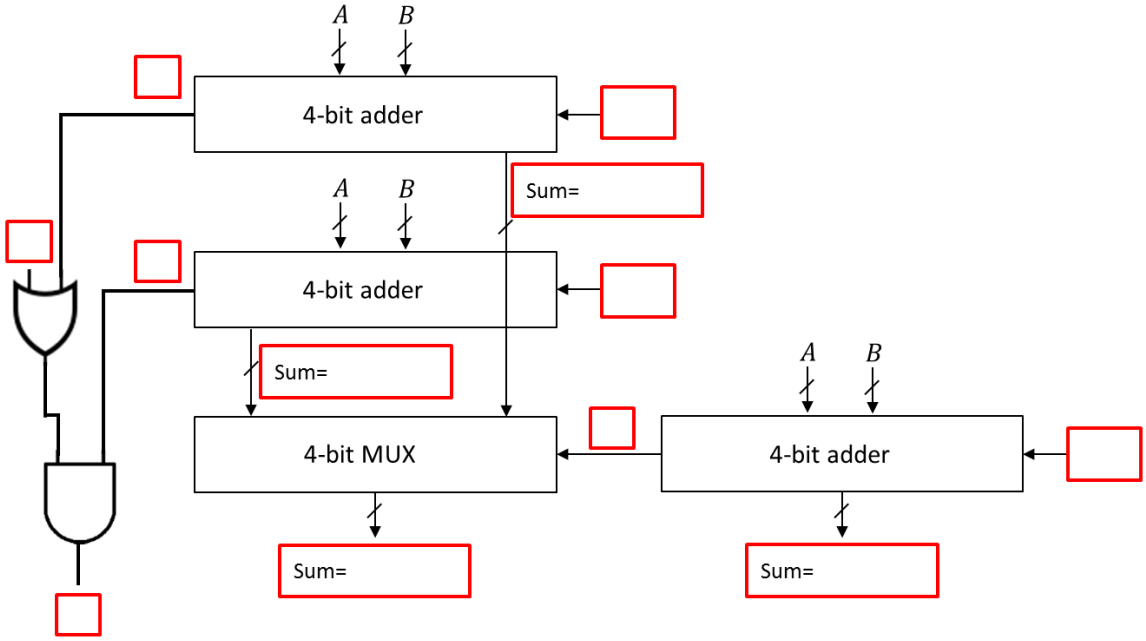
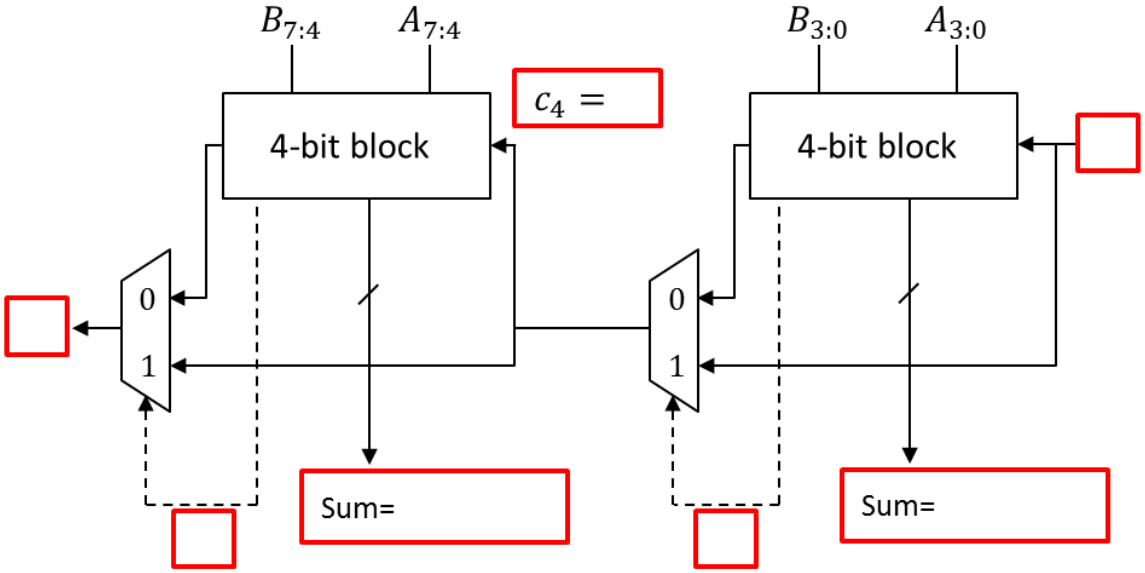
Homework Assignment 4
(Due Dec. 9, 11:59pm)

(1) **[Adder, 10 points]** Add the following three numbers using the carry select adder shown below. A=10101010, B=01010101, Cin=1 (Fill in the blank boxes).



(2) **[Adder, 10 points]** Add the following three numbers using the carry skip adder shown below. A=10101010, B=01010101, Cin=1 (Fill in the blank boxes).



(3) **[Adder, 10 points]** Add the following three numbers using the conditional sum adder shown below. A=11101110, B=01111001, Cin=1 (Fill in the blank boxes).

	i:	7	6	5	4	3	2	1	0
	A_i:	1	1	1	0	1	1	1	0
	B_i:	0	1	1	1	1	0	0	1
Step 1	S_i^0:								
	CO_i^0:								
	S_i^1:								
	CO_i^1:								
Step 2	S_i^0:								
	CO_i^0:								
	S_i^1:								
	CO_i^1:								
Step 3	S_i^0:								
	CO_i^0:								
	S_i^1:								
	CO_i^1:								
Result									

$CI_0 = 1$

(4) **[Adder, 20 points]** The delay of an AND (OR) gate is Δ and the delay of a two-level (sum-of-product) logic is 2Δ. We are designing a 1024-bit Kogge-Stone adder. Represent c_{87} hierarchically using group-generated and group-propagated carries ($g_{i:k}, p_{i:k}$) and c_0 (primary carry-in), then calculate the delay to obtain c_{87} assuming all the primary input signals are available at time 0.

(5) **[Adder, 20 points]** The delay of an AND (OR) gate is Δ and the delay of a two-level (sum-of-product) logic is 2Δ. We are designing a 1024-bit carry-lookahead adder. Represent c_{87} hierarchically using group-generated and group-propagated carries $(g_{i:k}, p_{i:k})$ and c_0 (primary carry-in), then calculate the delay to obtain c_{87} assuming all the primary input signals are available at time 0.