EE 434
Catalog Description:

ASIC architectures and design methods; digital systems and circuits; system test methods.

Semester: Spring 2018

Instructor: Dae Hyun Kim

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Office Hours: MWF 5:10-6pm or by appointment

TA: Dongjin Lee

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TA Office: Sloan 354

TA's office hours:

Credits: 3

Structure:

Three one-hour lectures per week, 3~5 lab assignments, 20~35 homework assignments, two midterm exams, and one final exam.

Topics:

(1) CMOS Circuit design methodologies: Different circuit design styles, comparative analysis. (6)

(2) Implementation methods: Custom & Semicustom design, Standard-cell based design, and Array based design, Layout, Place& Route, Power grid and clock design. (6)

(3) FPGA: Comparison between standard ASICs and FPGAs. Different FPGA families, their advantages and disadvantages (8)

(4) RTL design & synthesis: VHDL & Verilog. Design of Simple Processors, Network routers and other important Digital blocks. Emphasis on synthesis, Synthesis through scripts, use of Synopsys Design Compiler. (14)

(5) Design for Testability (DFT) techniques: Fault models, Fault equivalence, BIST, LFSR, MISR, Scan design, JTAG, IDDQ Test, SoC Test, P1500. (8)

Textbooks:

Other References:

(1) Analysis and Design of Digital Integrated Circuits by Hodges, Jackson and Saleh, Third Edition, McGraw hill, ISBN 0-07-228365-3

(2) Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. L. Bushnell and V. D. Agrawal, Boston: Springer, 2005, ISBN 0-7923-7991-8

(3) The Designer's Guide to VHDL by Peter J. Ashenden, Morgan Kaufmann, ISBN 1558606742

(4) Fundamentals of digital logic with verilog design by Brown & Vranesic, McGraw hill, ISBN 0-07-283878-7

Grading:

Homework Assignments	30%
Midterms	20% (10% each)
Lab Assignments	30%
Final Exam	20%

Late submission (homework): I will not accept any late submission. If you need more time, ask me by no later than 6 hours before the submission deadline. However, there should be a good reason for that (e.g., illness, a trip for a job interview, etc.).

Late submission (lab): I will not accept any late submission.

Assignments:

There will be a number of homework assignments and lab assignments. Students are expected to work individually on the homework assignments and the labs.

Reasonable accommodations are available for students who have a documented disability. Please notify the instructor during the first week of class of any

accommodations needed for the course. Late notification may cause the requested accommodations to be unavailable. All accommodations must be approved through the Disability Resource Center (DRC) in Administration Annex room 205, 335-1566, email:drc@mail.wsu.edu in Pullman.