Electronic Analysis of CMOS Logic Gates

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References

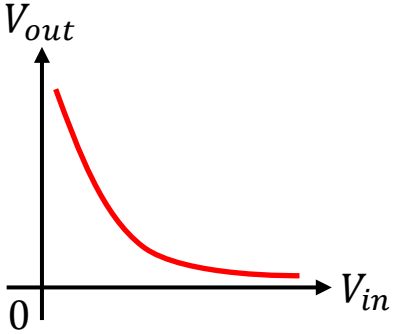
- John P. Uyemura, “Introduction to VLSI Circuits and Systems,” 2002.
  - Chapter 7

Goal

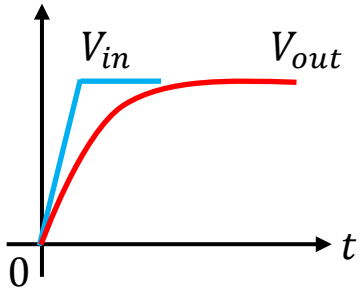
- Understand how to perform electronic analysis of CMOS logic gates.
  - DC characteristics
    - Noise margin
  - Switching characteristics
  - Power

Analysis

- DC Analysis
  - Vin vs. Vout = Voltage Transfer Characteristic (VTC)

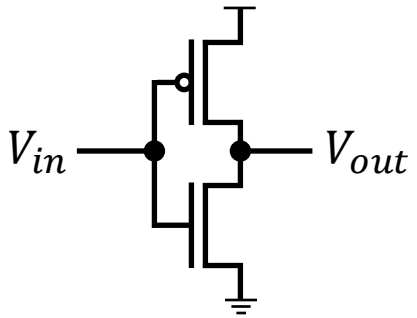


- Transient (switching) analysis
  - Vin(t) vs. Vout(t)



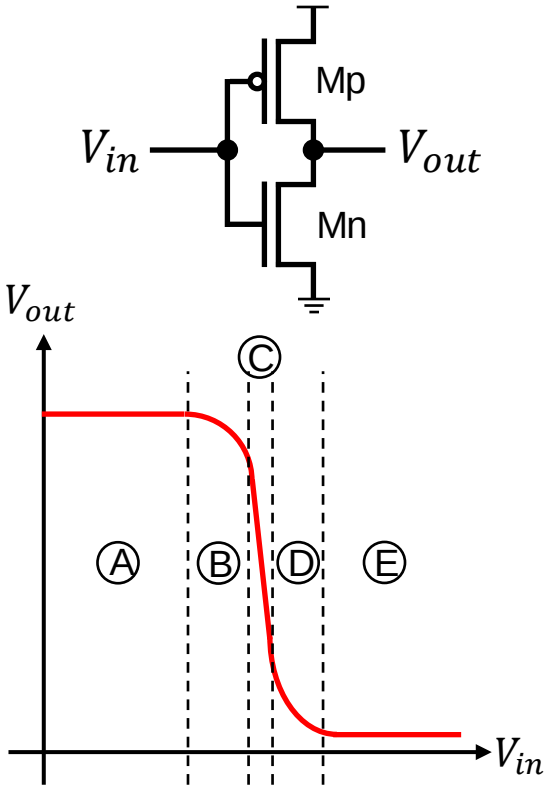
CMOS Inverter – DC Characteristics

- Logic swing
  - When $V_{in} = 0$
    - $V_{out} = V_{DD}$
    - Output high voltage $V_{OH} = V_{DD}$
  - When $V_{in} = V_{DD}$
    - $V_{out} = 0$
    - Output low voltage $V_{OL} = 0$
  - Logic swing
    - $V_L = V_{OH} - V_{OL} = V_{DD}$



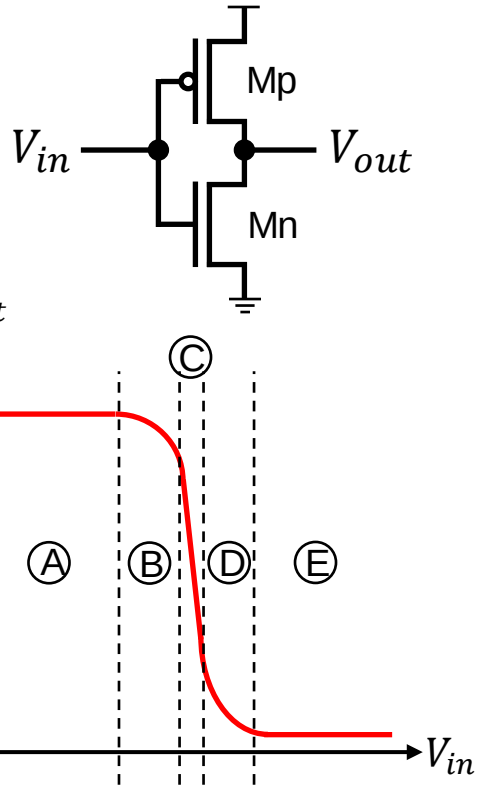
CMOS Inverter – DC Characteristics

- Region A ($0 \leq V_{in} \leq V_{Tn}$)
  - Mn
    - $V_{GSn} = V_{in} - 0 = V_{in}$
    - $V_{GSn} < V_{Tn}$: **Cut-off**
  - Mp
    - $V_{SGp} = V_{DD} - V_{in}$
    - $V_{SDp} = V_{DD} - V_{out}$
    - $(V_{SGp} - |V_{Tp}|) - V_{SDp} = V_{out} - V_{in} - |V_{Tp}| > 0$
    - $V_{SGp} - |V_{Tp}| > V_{SDp}$: **Linear**
  - $V_{out} \approx V_{DD}$



CMOS Inverter – DC Characteristics

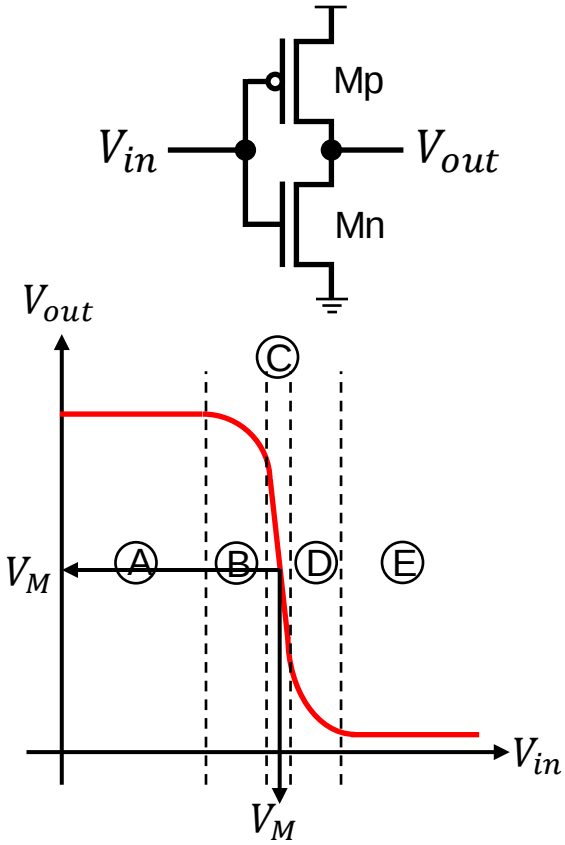
- Region B ($V_{Tn} \leq V_{in} < \frac{V_{DD}}{2}$)
  - Mn
    - $V_{GSn} - V_{Tn} = V_{in} - V_{Tn} > 0$
    - $V_{DSn} = V_{out}$
    - $(V_{GSn} - V_{Tn}) - V_{DSn} = V_{in} - V_{Tn} - V_{out} < 0$
    - $V_{GSn} - V_{Tn} < V_{DSn}$: **Saturation**
  - Mp
    - $V_{SGp} = V_{DD} - V_{in}$
    - $V_{SDp} = V_{DD} - V_{out}$
    - $\left(V_{SGp} - \left|V_{Tp}\right|\right) - V_{SDp} = V_{out} - V_{in} - \left|V_{Tp}\right| > 0$
    - $V_{SGp} - \left|V_{Tp}\right| > V_{SDp}$: **Linear**



  - $V_{out} = \left(V_{in} - \left|V_{Tp}\right|\right) + \sqrt{(V_{in} - |V_{Tp}|)^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - \left|V_{Tp}\right|\right)V_{DD} - \frac{\beta_n}{\beta_p}(V_{in} - V_{Tn})^2}$

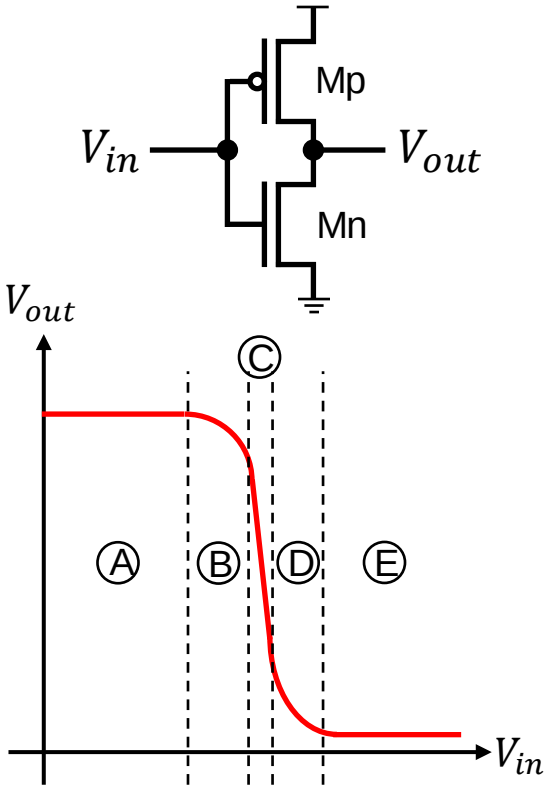
CMOS Inverter – DC Characteristics

- Region C ($V_{in} \approx \frac{V_{DD}}{2}$)
  - Mn
    - $(V_{GSn} - V_{Tn}) - V_{DSn} = V_{in} - V_{Tn} - V_{out} < 0$
    - $V_{GSn} - V_{Tn} < V_{DSn}$: **Saturation**
  - Mp
    - $(V_{SGp} - |V_{Tp}|) - V_{SDp} = V_{out} - V_{in} - |V_{Tp}| < 0$
    - $V_{SGp} - |V_{Tp}| < V_{SDp}$: **Saturation**
  - $I_{DSn} = \frac{\beta_n}{2}(V_M - V_{Tn})^2$
  - $I_{SDp} = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{Tp}|)^2$
  - Solve $I_{DSn} = I_{SDp}$.
  - $V_M = \frac{V_{DD} - |V_{Tp}| + V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$



CMOS Inverter – DC Characteristics

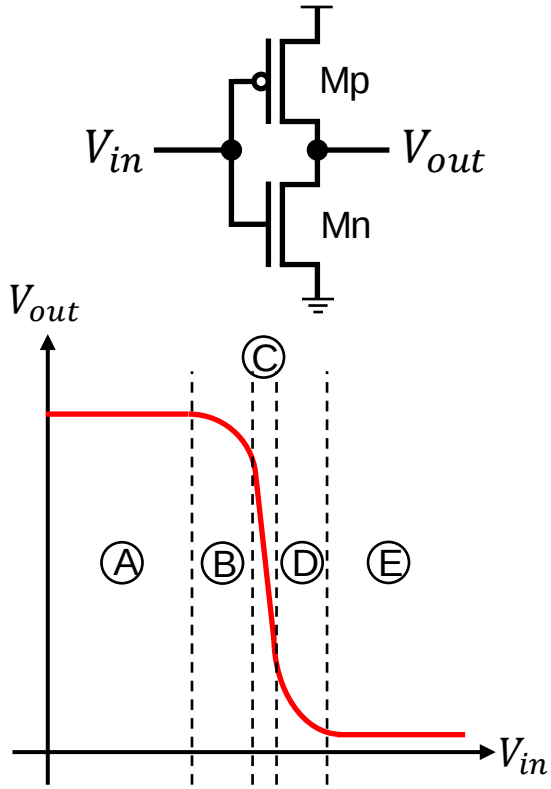
- Region D ($\frac{V_{DD}}{2} < V_{in} \leq V_{DD} - |V_{Tp}|$)
  - Mn
    - $V_{GSn} - V_{Tn} = V_{in} - V_{Tn} > 0$
    - $V_{DSn} = V_{out}$
    - $(V_{GSn} - V_{Tn}) - V_{DSn} = V_{in} - V_{Tn} - V_{out} > 0$
    - $V_{GSn} - V_{Tn} > V_{DSn}$: **Linear**
  - Mp
    - $V_{SGp} = V_{DD} - V_{in}$
    - $V_{SDp} = V_{DD} - V_{out}$
    - $(V_{SGp} - |V_{Tp}|) - V_{SDp} = V_{out} - V_{in} - |V_{Tp}| < 0$
    - $V_{SGp} - |V_{Tp}| < V_{SDp}$: **Saturation**



  - $V_{out} = (V_{in} - V_{Tn}) - \sqrt{(V_{in} - V_{Tn})^2 - \frac{\beta_p}{\beta_n}(V_{in} - V_{DD} - |V_{Tp}|)^2}$

CMOS Inverter – DC Characteristics

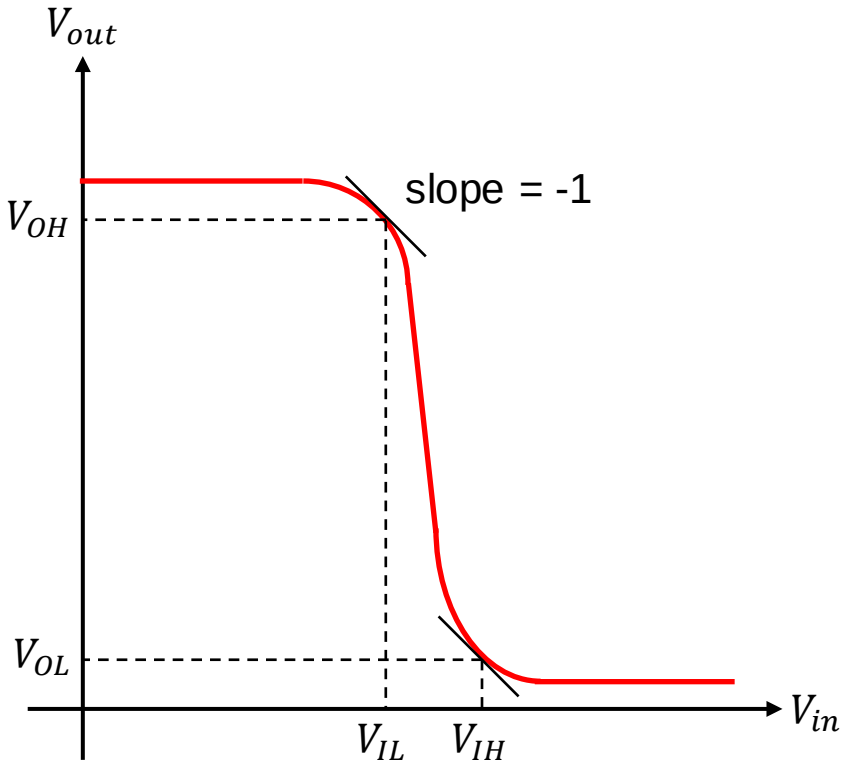
- Region E ($V_{DD} - |V_{Tp}| \leq V_{in} \leq V_{DD}$)
  - Mn
    - $V_{GSn} - V_{Tn} = V_{in} - V_{Tn} > 0$
    - $V_{DSn} = V_{out}$
    - $(V_{GSn} - V_{Tn}) - V_{DSn} = V_{in} - V_{Tn} - V_{out} > 0$
    - $V_{GSn} - V_{Tn} > V_{DSn}$: **Linear**
  - Mp
    - $V_{SGp} = V_{DD} - V_{in}$
    - $V_{SGp} - |V_{Tp}| < 0$: **Cut-off**
  - $V_{out} \approx 0$



CMOS Inverter – DC Characteristics

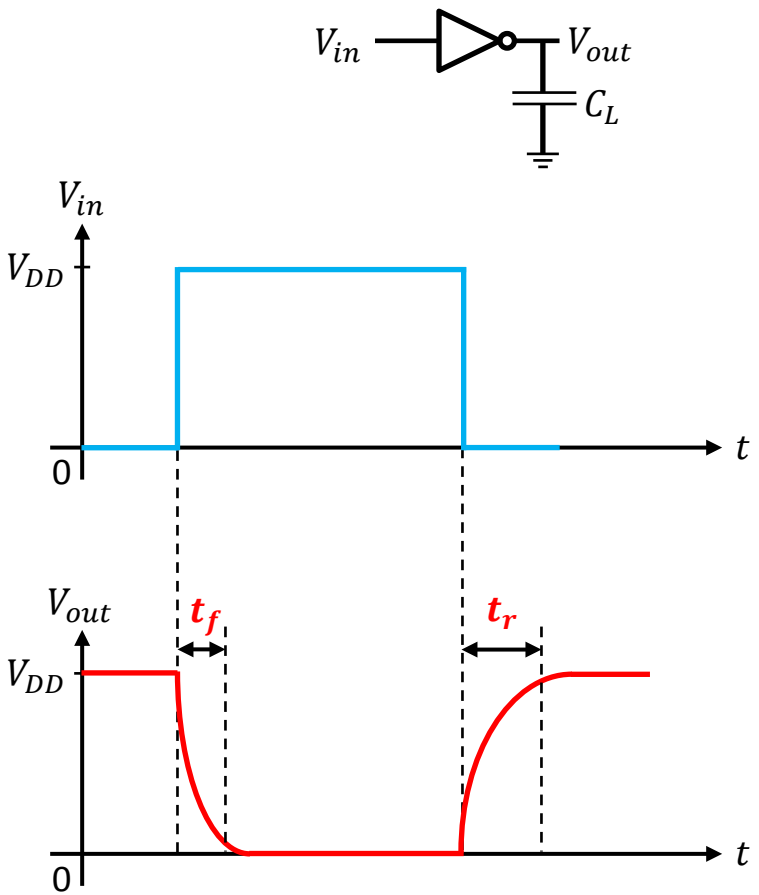
- Voltage noise margin
  - $VNM_H = V_{OH} - V_{IH}$
  - $VNM_L = V_{IL} - V_{OL}$

- V_{IH}: Min. high input voltage
- V_{IL}: Max. low input voltage
- V_{OH}: Min. high output voltage
- V_{OL}: Max. low output voltage



CMOS Inverter – Switching Characteristics

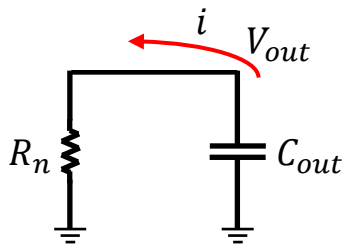
- t_r: rise time
- t_f: fall time
- C_{out}: total output capacitance
  - $C_{out} = C_{FET} + C_L$
    - C_{FET}: FET capacitance
      - $C_{FET} = C_{Dn} + C_{Dp}$
        - » $C_{Dn} = C_{GSn} + C_{DBn}$
        - » $C_{Dp} = C_{GSp} + C_{DBp}$
    - C_L: load capacitance



CMOS Inverter – Switching Characteristics

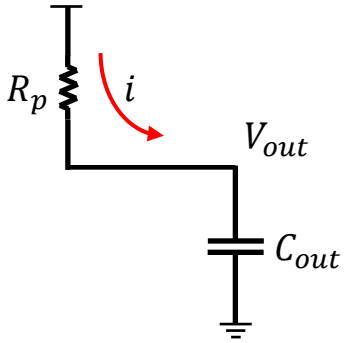
- Fall time
  - From $V_{out} = 0.9V_{DD}$ to $V_{out} = 0.1V_{DD}$

- Fall time calculation
  - Discharging (Natural response)
  - $i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$
    - $R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})}$
  - $V_{out}(t) = V_{DD}e^{-\frac{t}{\tau_n}}$
    - $\tau_n = R_n C_{out}$ (time constant)
  - $t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$
  - $t_f = t(V_{out} = 0.1V_{DD}) - t(V_{out} = 0.9V_{DD}) = \tau_n\left(\ln 10 - \ln\frac{10}{9}\right) = \tau_n \ln 9$
  - $t_f \approx 2.2\tau_n$
  - $t_{HL} = t_f$
    - t_{HL}: high-to-low time



CMOS Inverter – Switching Characteristics

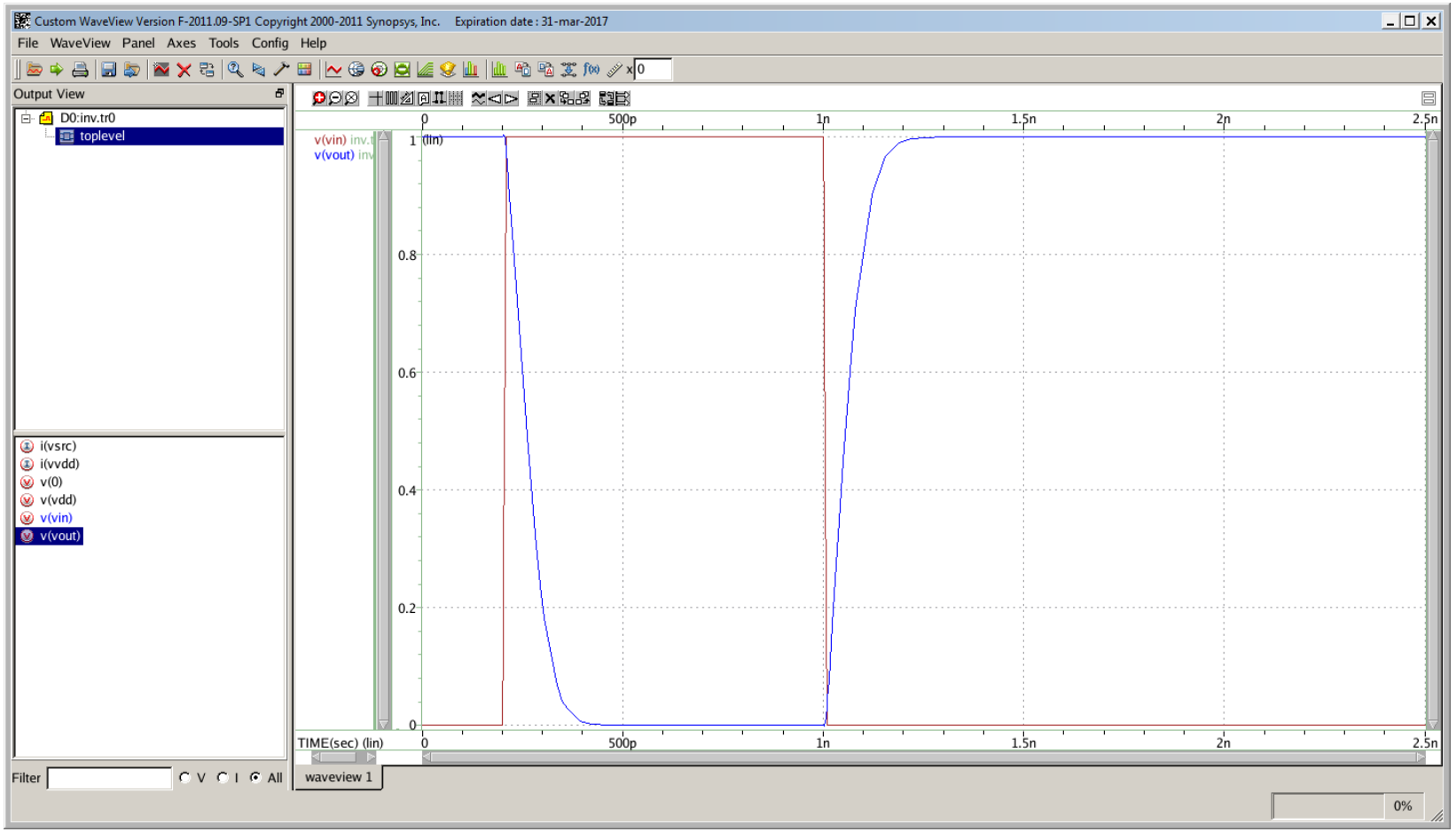
- Rise time
  - From $V_{out} = 0.1V_{DD}$ to $V_{out} = 0.9V_{DD}$



- Rise time calculation
  - Charging (Step response)
  - $i = C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD}-V_{out}}{R_p}$
    - $R_p = \frac{1}{\beta_p(V_{DD}-|V_{Tp}|)}$
  - $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{\tau_p}}\right)$
    - $\tau_p = R_pC_{out}$ (time constant)
  - $t = \tau_p \ln\left(\frac{V_{DD}}{V_{DD}-V_{out}}\right)$
  - $t_r = t(V_{out} = 0.9V_{DD}) - t(V_{out} = 0.1V_{DD}) = \tau_p\left(\ln 10 - \ln\frac{10}{9}\right) = \tau_p \ln 9$
  - $t_r \approx 2.2\tau_p$
  - $t_{LH} = t_r$
    - t_{LH}: low-to-high time

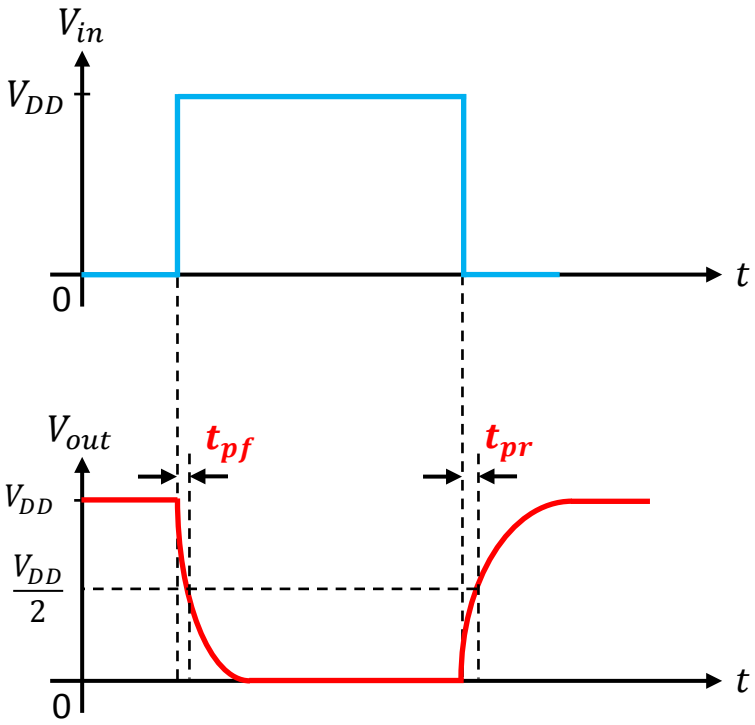
CMOS Inverter – Switching Characteristics

- Transient simulation of a CMOS inverter



CMOS Inverter – Switching Characteristics

- Maximum signal frequency
  - The largest frequency
  - $f_{max} = \frac{1}{t_{HL}+t_{LH}} = \frac{1}{t_f+t_r} = \frac{1}{2.2\,(\tau_n+\tau_p)}$
  - Example
    - $R_n = R_p = 500\Omega$
    - $C_{out} = 10fF$
    - $f_{max} = \frac{1}{2.2(5ps+5ps)} \approx 45GHz$
- Propagation delay
  - Delay time from input to output
  - $t_p = \frac{t_{pf}+t_{pr}}{2}$
    - t_{pf}: output fall time $(V_{DD} \rightarrow \frac{V_{DD}}{2})$
      - $t_{pf} = \tau_n \ln 2$
    - t_{pr}: output rise time $(0 \rightarrow \frac{V_{DD}}{2})$
      - $t_{pr} = \tau_p \ln 2$



CMOS Inverter – General Analysis

- Output capacitance
  - $C_{out} = C_{FET} + C_L$
- Rise time
  - $t_r = \tau_p \ln 9 \approx 2.2 R_p (C_{FET} + C_L) = t_{r0} + 2.2 R_p C_L$
    - $R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}$
- Fall time
  - $t_f = \tau_n \ln 9 \approx 2.2 R_n (C_{FET} + C_L) = t_{f0} + 2.2 R_n C_L$
    - $R_n = \frac{1}{\beta_n (V_{DD} - V_{Tp})}$
- Speed vs. area
  - $\beta \uparrow \implies R \downarrow \implies t \downarrow$
    - Area goes up, but the logic is faster.

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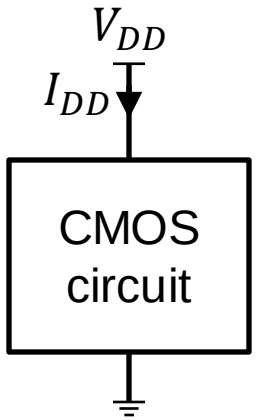
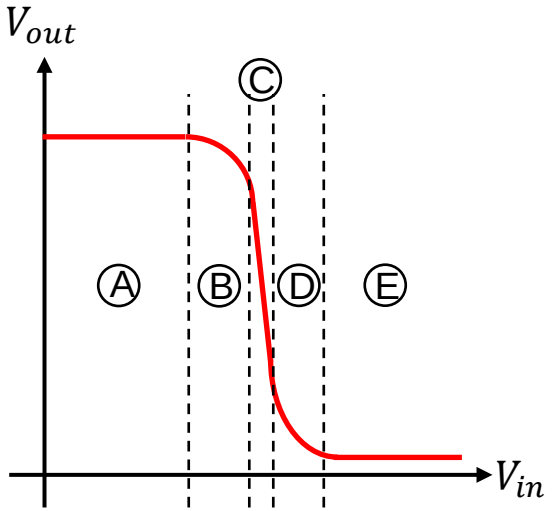
CMOS Inverter – Power Dissipation

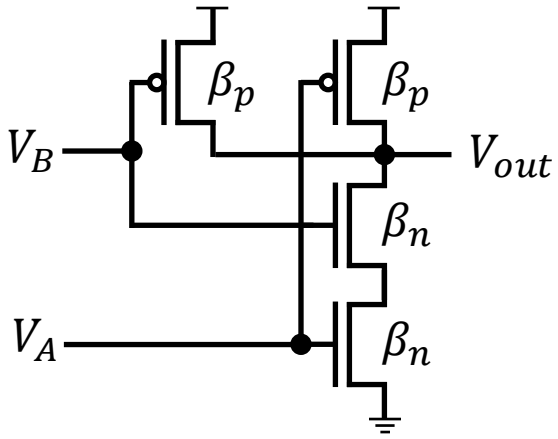
- Power dissipation calculation
  - $P = V_{DD} I_{DD}$
- $P = P_{DC} + P_{dyn}$
  - P_{DC}: DC power
    - Region A, E: $I_{DD} = 0$
      - Actually, there is leakage current I_{DDQ}.
        - » I_{DDQ}: quiescent leakage current
      - $P_{DC} = V_{DD} I_{DDQ}$
  - P_{dyn}: Dynamic power
    - Charging/Discharging
      - $Q_e = C_{out} V_{DD}$
    - $P = V_{DD} I_{DD} = V_{DD} \left(\frac{Q_e}{T}\right) = f C_{out} {V_{DD}}^2$
- $\boxed{P = V_{DD} I_{DDQ} + f C_{out} {V_{DD}}^2}$



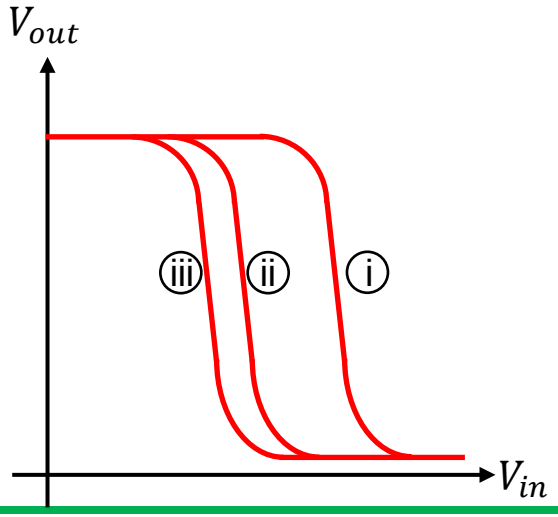


NAND2 – DC Characteristics

- $V_{Tn,B}$ goes up.

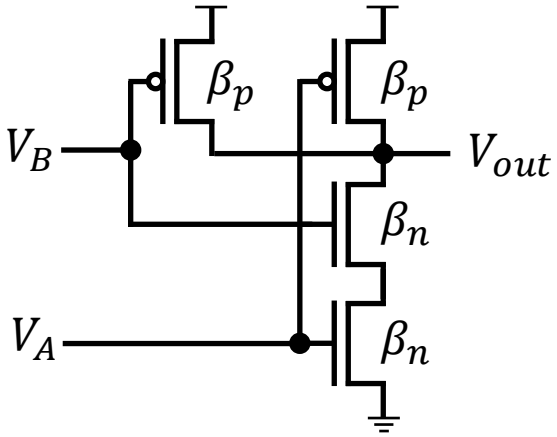


	V_A	V_B
(i)	$0 \rightarrow V_{DD}$	$0 \rightarrow V_{DD}$
(ii)	V_{DD}	$0 \rightarrow V_{DD}$
(iii)	$0 \rightarrow V_{DD}$	V_{DD}



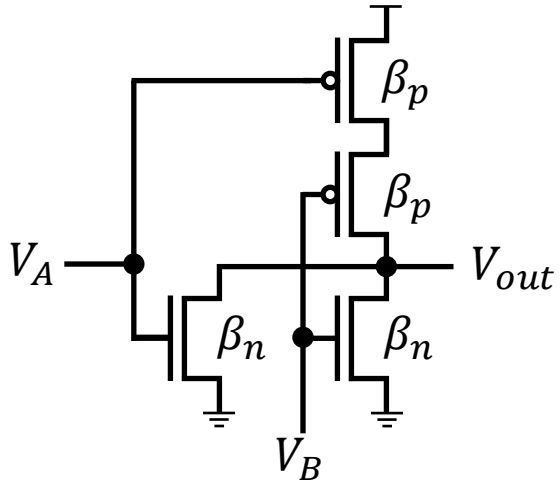
NAND2 – DC Characteristics

- V_M $(V_{in} = V_{out} = V_M)$
  - nFET network: $\frac{\beta_n}{2}$
  - pFET network: $2\beta_p$
  - Mn (V_A): $(V_{GSn} - V_{Tn}) - V_{DSn} = (V_M - V_{Tn}) - (< V_M) < 0$: **Saturation**
  - Mn (V_B): $(V_{GSn} - V_{Tn}) - V_{DSn} = (V_M - V_S - V_{Tn}) - (V_M - V_S) < 0$: **Saturation**
  - Mp: $\left(V_{SGp} - \left|V_{Tp}\right|\right) - V_{SDp} = \left(V_{DD} - V_M - \left|V_{Tp}\right|\right) - (V_{DD} - V_M) < 0$: **Saturation**
  - $I_{DSn} = \frac{(\frac{\beta_n}{2})}{2}(V_M - V_{Tn})^2$
  - $I_{SDp} = \frac{(2\beta_p)}{2}(V_{DD} - V_M - |V_{Tp}|)^2$
  - Solve $I_{DSn} = I_{SDp}$.
  - $V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{2}V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}}$
- For NAND*k*
  - $V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{k}V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{k}\sqrt{\frac{\beta_n}{\beta_p}}}$

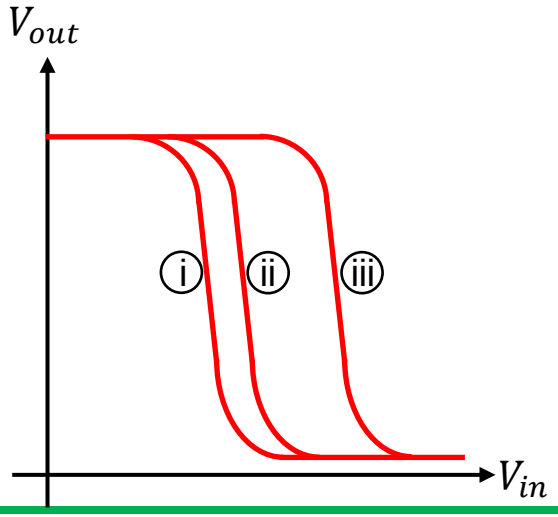


NOR2 – DC Characteristics

- $|V_{Tp,B}|$ goes up.

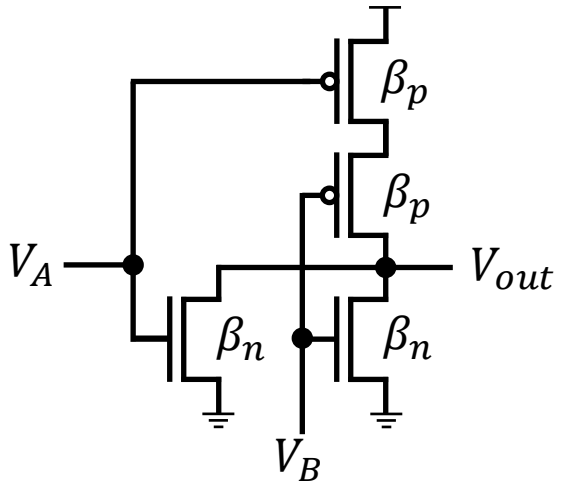


	V_A	V_B
(i)	$0 \rightarrow V_{DD}$	$0 \rightarrow V_{DD}$
(ii)	0	$0 \rightarrow V_{DD}$
(iii)	$0 \rightarrow V_{DD}$	0



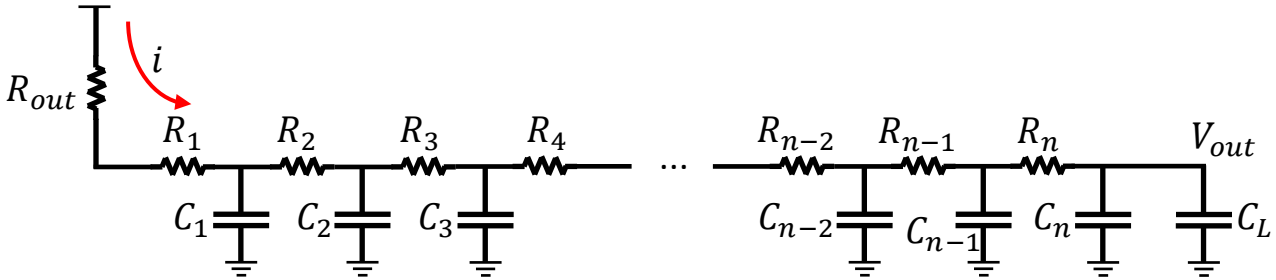
NOR2 – DC Characteristics

- V_M $(V_{in} = V_{out} = V_M)$
  - nFET network: $2\beta_n$
  - pFET network: $\frac{\beta_p}{2}$
  - Mn: $(V_{GSn} - V_{Tn}) - V_{DSn} = (V_M - V_{Tn}) - V_M < 0$: **Saturation**
  - Mp (V_A): $(V_{SGp} - |V_{Tp}|) - V_{SDp} = (V_{DD} - V_M - |V_{Tp}|) - (V_{DD} - V_M) < 0$: **Saturation**
  - Mp (V_B): $(V_{SGp} - |V_{Tp}|) - V_{SDp} = (V_S - V_M - |V_{Tp}|) - (V_S - V_M) < 0$: **Saturation**
  - $I_{DSn} = \frac{2\beta_n}{2}(V_M - V_{Tn})^2$
  - $I_{SDp} = \frac{(\frac{\beta_p}{2})}{2}(V_{DD} - V_M - |V_{Tp}|)^2$
  - Solve $I_{DSn} = I_{SDp}$.
  - $V_M = \frac{V_{DD} - |V_{Tp}| + 2V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + 2\sqrt{\frac{\beta_n}{\beta_p}}}$
- For NOR*k*
  - $V_M = \frac{V_{DD} - |V_{Tp}| + kV_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + k\sqrt{\frac{\beta_n}{\beta_p}}}$



Elmore Delay

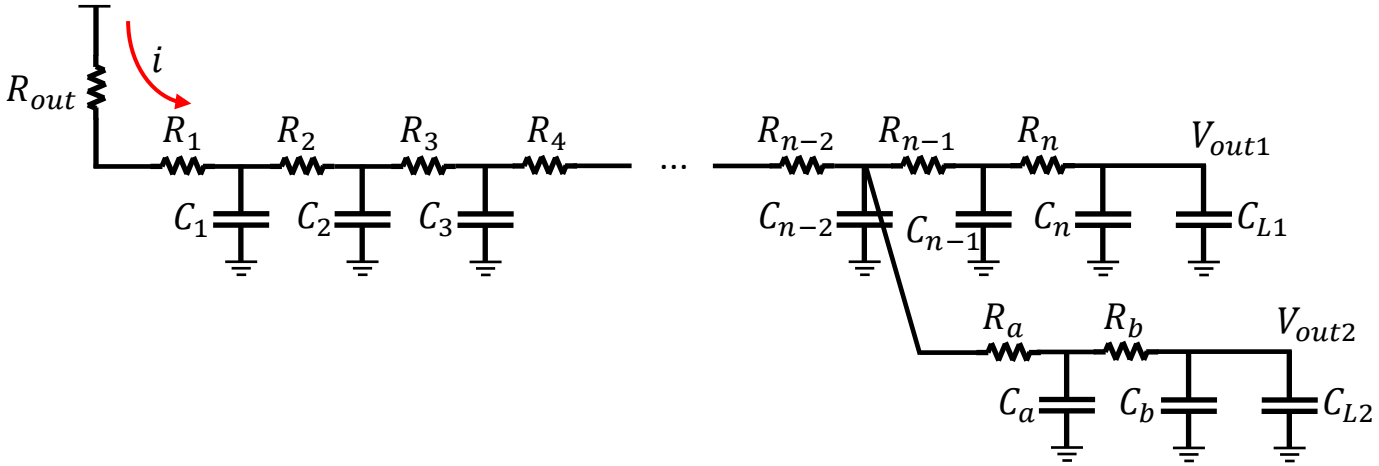
- How to estimate delay in general RC networks.
  - How to
    - Start at the target sink node.
    - Traverse the RC network toward the source.
    - Whenever there is a resistor, multiply its resistance and its downstream capacitance and add it to the total delay.
  - For two-pin nets



$$\tau = R_n(C_n + C_L) + R_{n-1}(C_{n-1} + C_n + C_L) + R_{n-2}(C_{n-2} + C_{n-1} + C_n + C_L) + \ldots + R_3(C_3 + \cdots + C_n + C_L) + R_2(C_2 + \cdots + C_n + C_L) + R_1(C_1 + \cdots + C_n + C_L) + R_{out}(C_1 + \cdots + C_n + C_L)$$

Elmore Delay

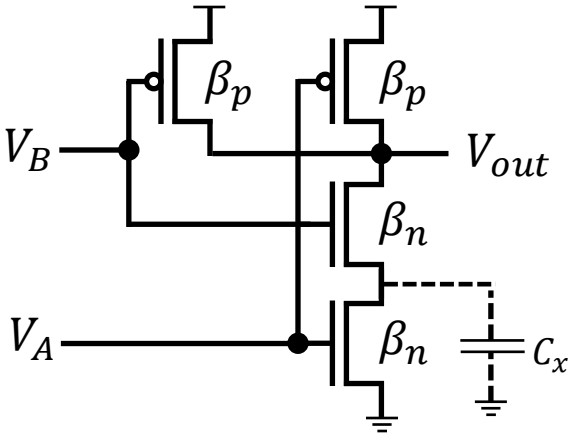
- How to estimate delay in general RC networks.
  - For multi-pin nets



$$\tau(V_{out1}) = R_n(C_n + C_{L1}) + R_{n-1}(C_{n-1} + C_n + C_{L1}) +$$
$$R_{n-2}(C_{n-2} + C_{n-1} + C_n + C_{L1} + C_a + C_b + C_{L2}) +$$
$$\ldots + R_3(C_3 + \cdots + C_n + C_{L1} + C_a + C_b + C_{L2}) +$$
$$R_2(C_2 + \cdots + C_n + C_{L1} + +C_a + C_b + C_{L2}) + R_1(C_1 + \cdots + C_n + C_{L1} + C_a + C_b + C_{L2}) +$$
$$R_{out}(C_1 + \cdots + C_n + C_{L1} + +C_a + C_b + C_{L2})$$

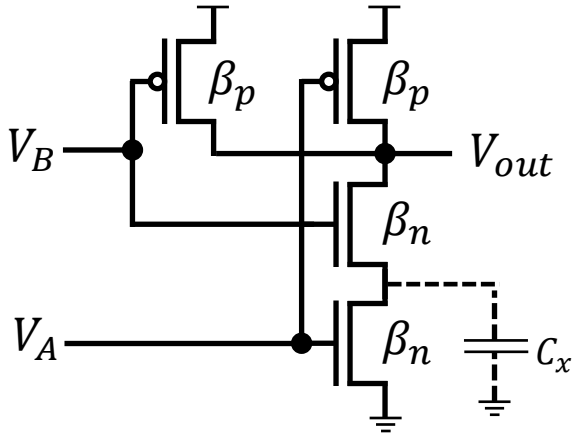
NAND2 – Switching Characteristics

- t_r: rise time
- t_f: fall time
- C_{out}: total output capacitance
  - $C_{out} = C_{FET} + C_L$
    - C_{FET}: FET capacitance
      - $C_{FET} = C_{Dn} + 2C_{Dp}$
        - » $C_{Dn} = C_{GSn} + C_{DBn}$
        - » $C_{Dp} = C_{GSp} + C_{DBp}$
    - C_L: load capacitance
  - C_x: parasitic capacitance



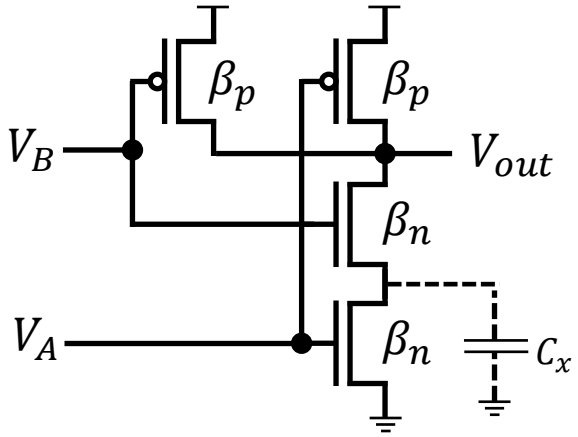
NAND2 – Switching Characteristics

- Rise time
  - If $AB: 11 \rightarrow 00$ (best case)
    - $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{\tau_p}}\right)$
      - $\tau_p = \frac{R_p}{2} C_{out}$
    - $t_r \approx 2.2\tau_p$
  - If $AB: 11 \rightarrow 10$ or $AB: 11 \rightarrow 01$ (worst case)
    - $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{\tau_p}}\right)$
      - $\tau_p = R_p C_{out}$
    - $t_r \approx 2.2\tau_p$
  - $t_r = 2.2R_p(C_{FET} + C_L)$



NAND2 – Switching Characteristics

- Fall time
  - If $AB: 00 \rightarrow 11$ or $AB: 10 \rightarrow 11$ (best case)
    - $V_{out}(t) = V_{DD} e^{-\frac{t}{\tau_n}}$
      - $\tau_n = 2R_n C_{out}$
    - $t_f \approx 2.2\tau_n$
  - If $AB: 01 \rightarrow 11$ (worst case)
    - $V_{out}(t) = V_{DD} e^{-\frac{t}{\tau_n}}$
      - $\tau_n = 2R_n C_{out} + R_n C_x$
    - $t_f \approx 2.2\tau_n$
  - $t_f = 2.2[2R_n(C_{FET} + C_L)] + 2.2R_n C_x$



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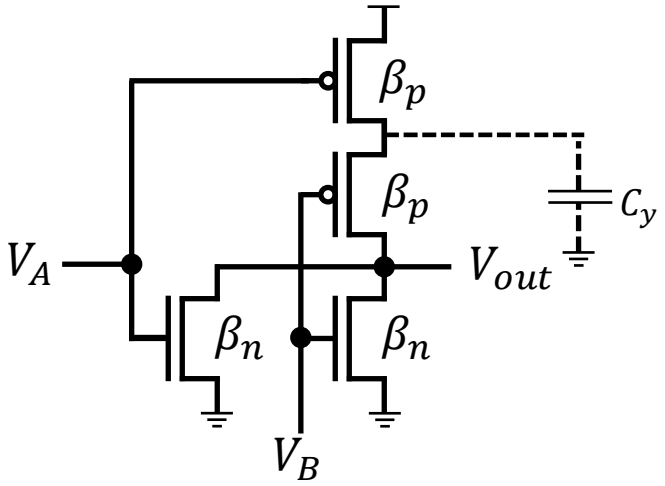
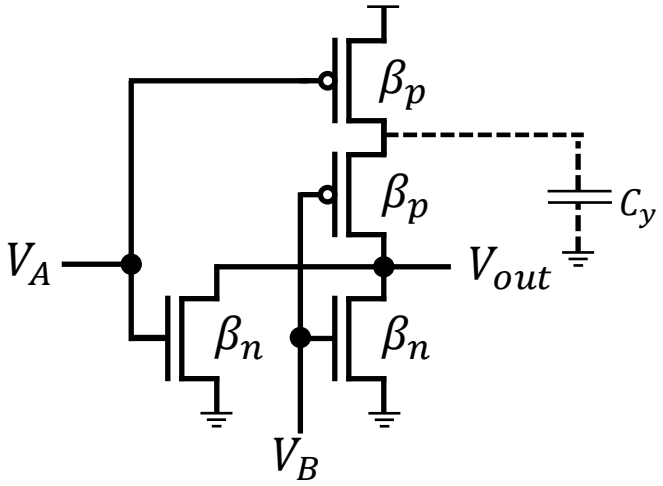
NOR2 – Switching Characteristics

- t_r: rise time
- t_f: fall time
- C_{out}: total output capacitance
  - $C_{out} = C_{FET} + C_L$
    - C_{FET}: FET capacitance
      - $C_{FET} = 2C_{Dn} + C_{Dp}$
        - » $C_{Dn} = C_{GSn} + C_{DBn}$
        - » $C_{Dp} = C_{GSp} + C_{DBp}$
    - C_L: load capacitance
  - C_x: parasitic capacitance



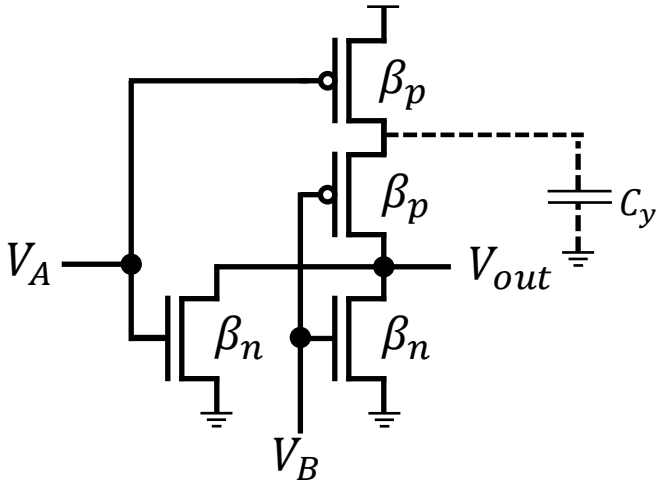
NOR2 – Switching Characteristics

- Fall time
  - If $AB: 00 \rightarrow 11$ (best case)
    - $V_{out}(t) = V_{DD} e^{-\frac{t}{\tau_n}}$
      - $\tau_n = \frac{R_n}{2} C_{out}$
    - $t_f \approx 2.2\tau_n$
  - If $AB: 00 \rightarrow 10$ or $AB: 00 \rightarrow 01$ (worst case)
    - $V_{out}(t) = V_{DD} e^{-\frac{t}{\tau_n}}$
      - $\tau_n = R_n C_{out}$
    - $t_f \approx 2.2\tau_n$
  - $t_f = 2.2 R_n C_{out}$



NOR2 – Switching Characteristics

- Rise time
  - If $AB: 01 \rightarrow 00$ (best case)
    - $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{\tau_p}}\right)$
      - $\tau_p = 2R_pC_{out}$
    - $t_r \approx 2.2\tau_p$
  - If $AB: 10 \rightarrow 00$ or $AB: 11 \rightarrow 00$ (worst case)
    - $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{\tau_p}}\right)$
      - $\tau_p = 2R_pC_{out} + R_pC_y$
    - $t_r \approx 2.2\tau_p$
  - $t_r = 2.2[2R_p(C_{FET} + C_L)] + 2.2R_pC_y$



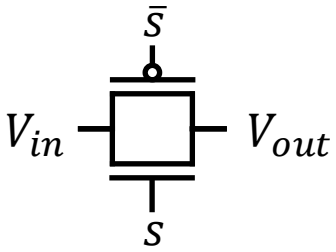
Power Dissipation

- Dynamic power
  - $P_{dyn} = \alpha f C {V_{DD}}^2$
    - α: switching activity
    - f: clock frequency
    - C: capacitance

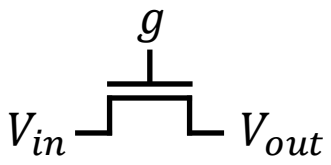
- More accurate formula
  - $P_{dyn} = f {V_{DD}}^2 \sum_{i=1}^{n} \alpha_i C_i$

Transmission Gates and Pass Transistors

- Transmission gates
  - Approximation
    - $R_{TG} = \max(R_n, R_p)$
    - $C_{in} = C_{nFET,source} + C_{pFET,drain}$



- Pass transistors
  - Rise time
    - $t_r = 18R_nC_{out}$
  - Fall time
    - $t_f = 2.94R_nC_{out}$



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