EE 434
ASIC and Digital Systems

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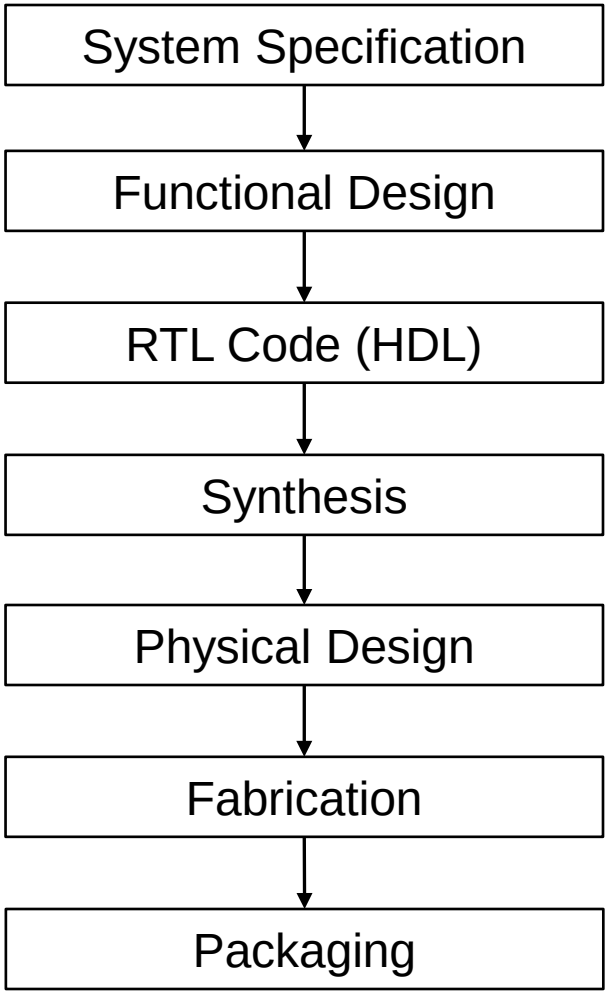
School of Electrical Engineering and Computer Science
Washington State University

Preliminaries

VLSI Design



Freq Area Power

64-bit integer multiplier / 1GHz / 0.1mm^2 / 0.1mW

C/C++, Verilog, VHDL, …

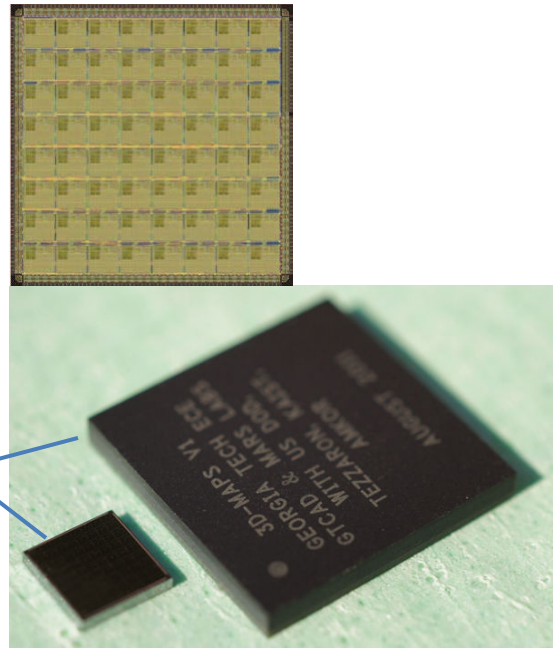
```
module imul_64 (a, b, clk, out64);
input a, b, clk;  output out64; … endmodule
```

Netlist

Layout

Bare die

Chip

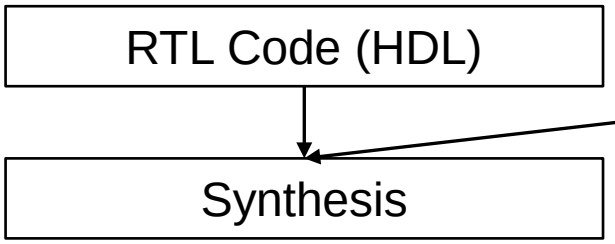


From RTL Code to a Chip

RTL Code (HDL)

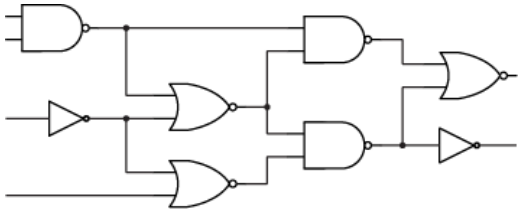
```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  reg [63:0] int_stage1;
  reg [63:0] int_stage2;

  always @ (posedge clk)
  begin
    ...
  end

endmodule
```

From RTL Code to a Chip



Tech library
(e.g., 45nm)

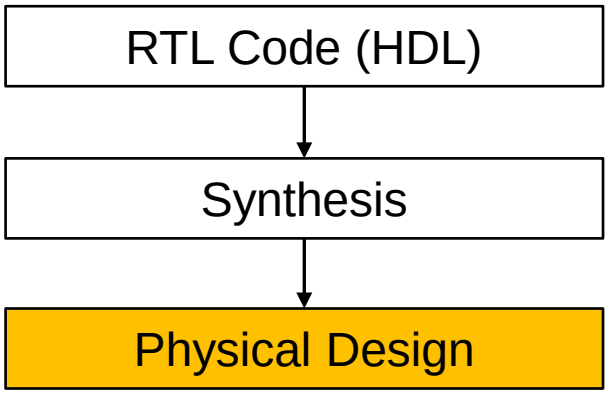
```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  reg [63:0] int_stage1;
  reg [63:0] int_stage2;

  always @ (posedge clk)
  begin
    ...
  end

endmodule
```

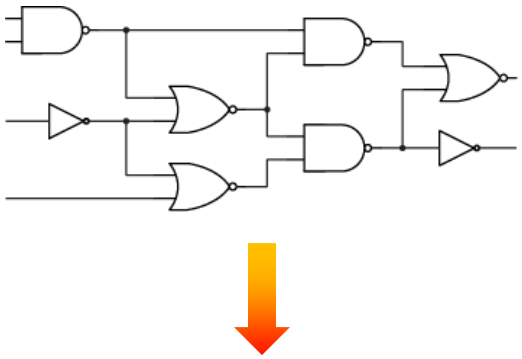


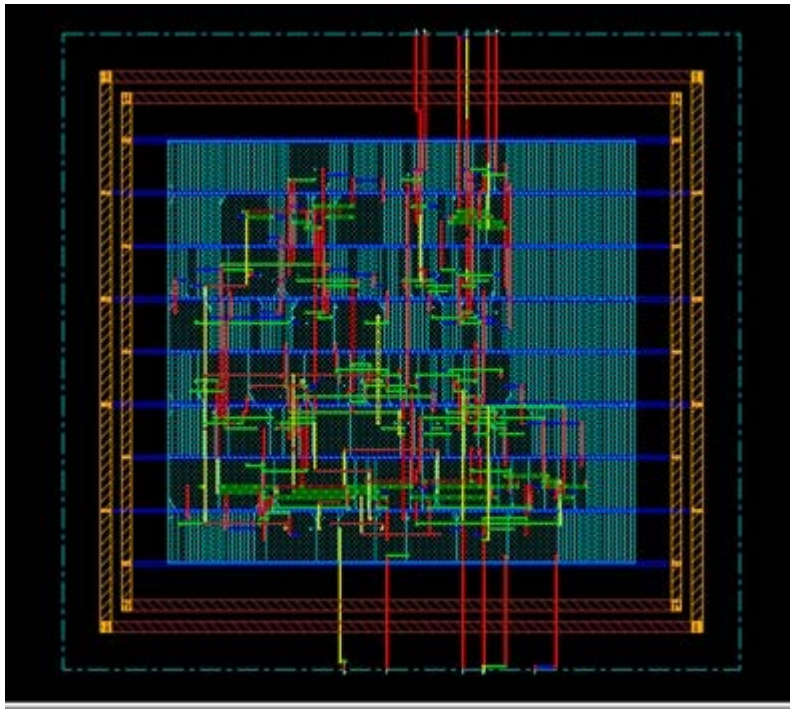
Tech-specific logic gates

```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  NAND2_X1 ( .A(in_1[0]), .B(in_2[0]), .Z(n1) );
  FA_X1 ( .A(in_1[0]), .B(in_2[0]), .CI(1'b0), .S(n2), .CO(n3) );
  ...

endmodule
```

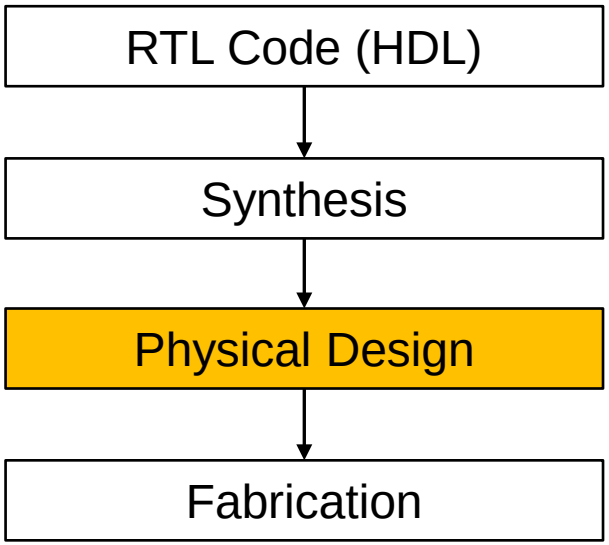
From RTL Code to a Chip

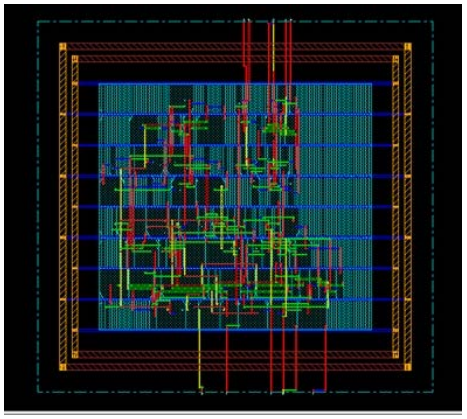


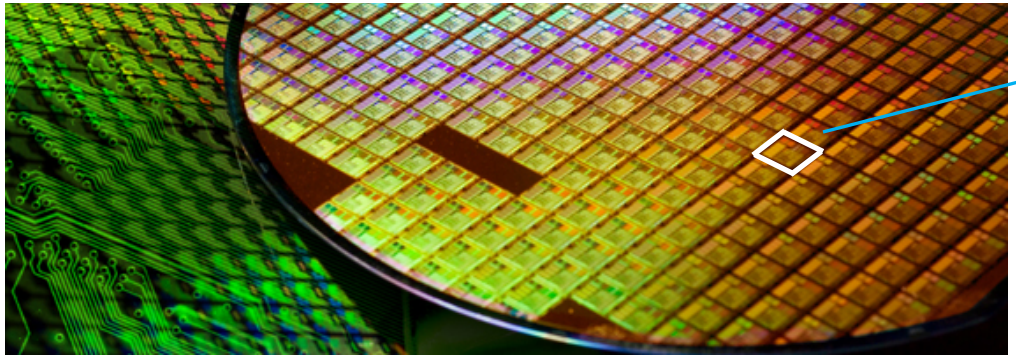


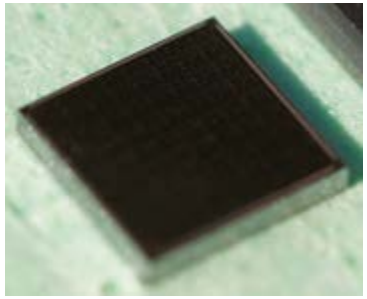


From RTL Code to a Chip

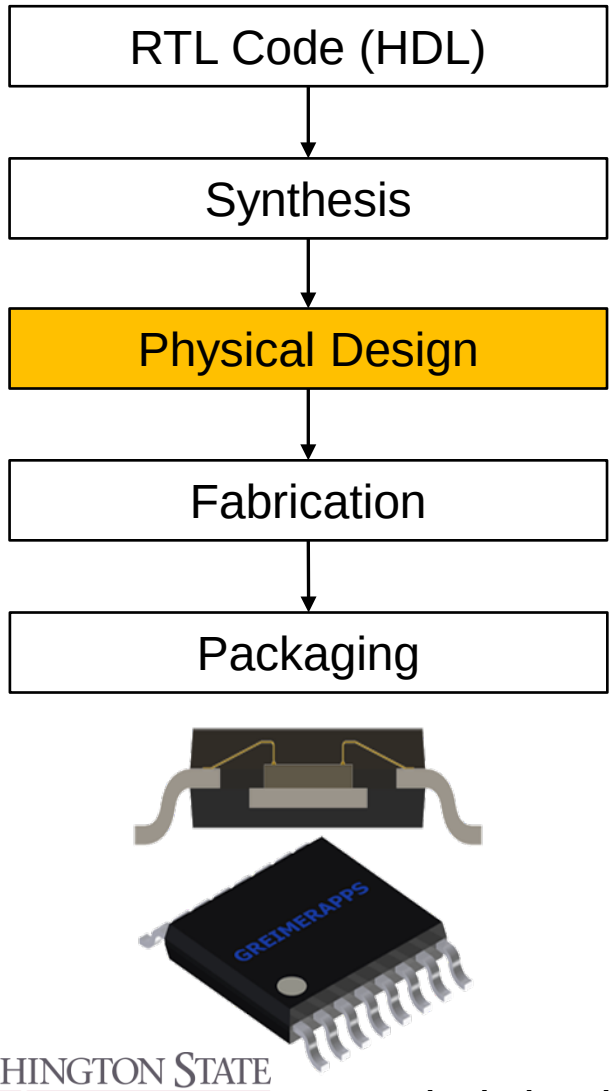


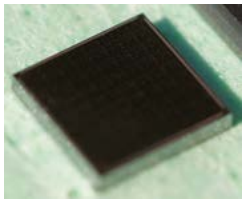


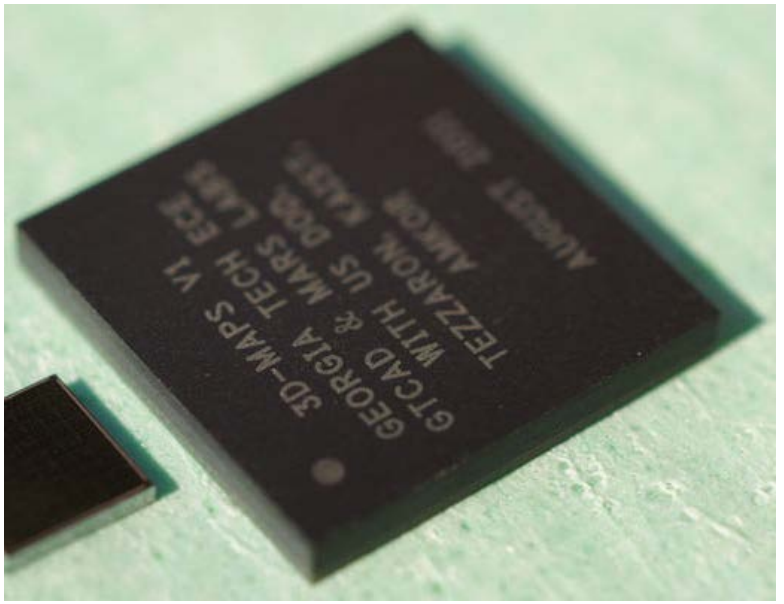




From RTL Code to a Chip

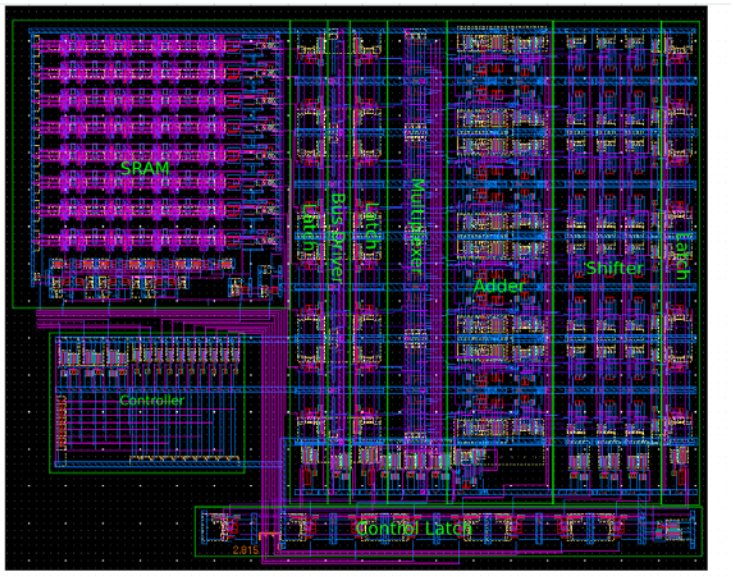


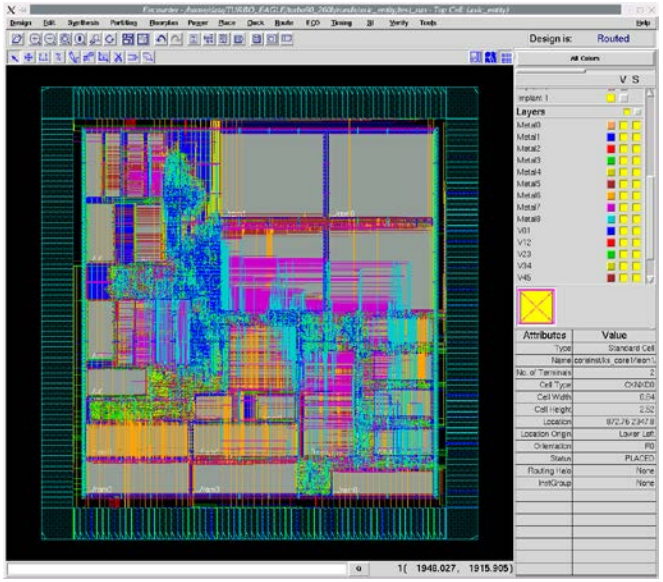




VLSI Design

	Full custom	ASIC
Design	Manual	Automatic
TRs	Manually drawn	Standard-cell based
Placement & Routing	Custom	Automatic
Development time	Several months	A few days ~ weeks





Standard-Cell-Based Design

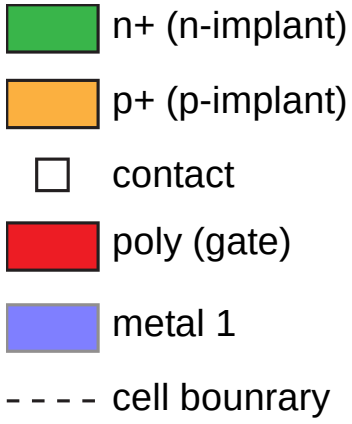
- Provides
  - good performance
  - low power
  - small area
  - …
- Other design styles
  - FPGA
  - PLA
  - …

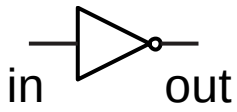
Standard-Cell-Based Design

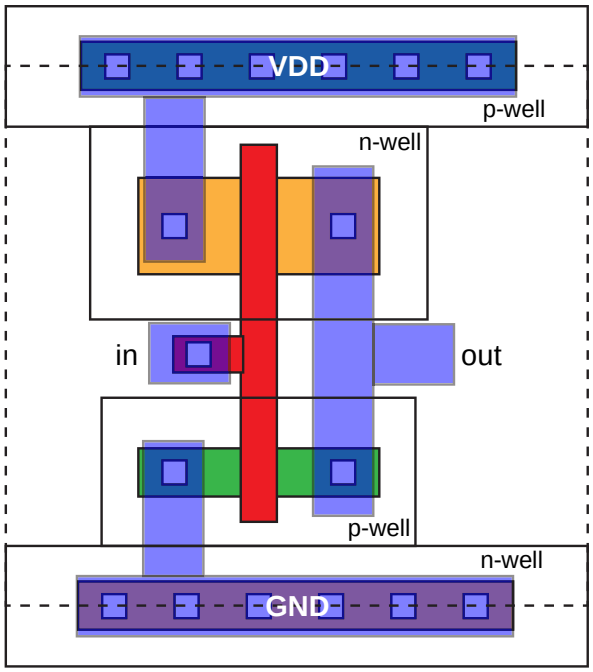
- Standard cells
  - A set of logic gates
  - Have the same height.
  - Width varies.
  - Pre-characterized for timing and power analysis.

INV NAND2

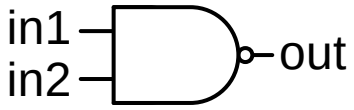
Standard Cells (Layout)

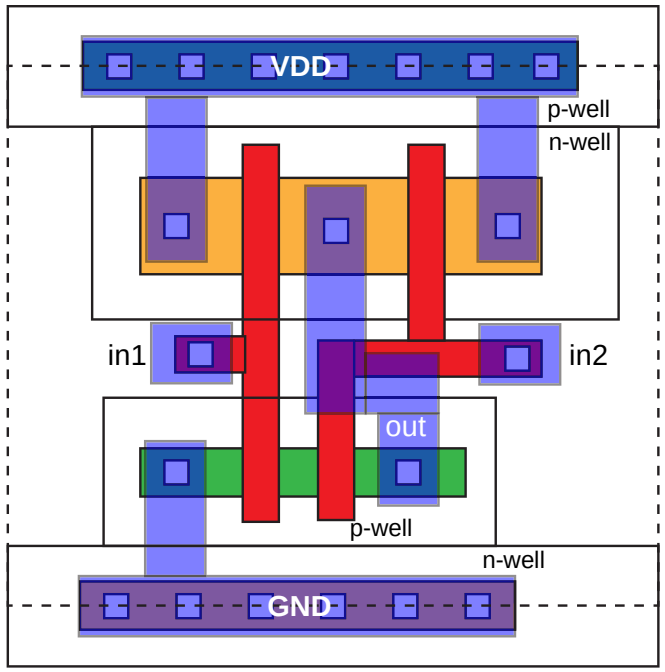






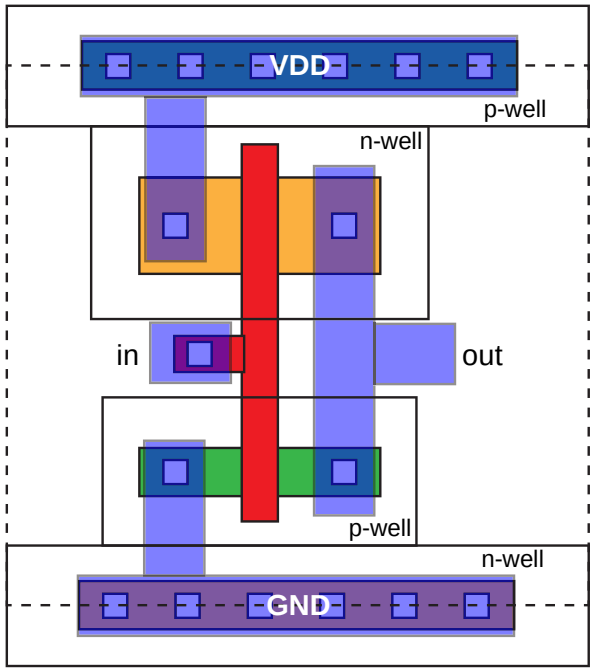
INV



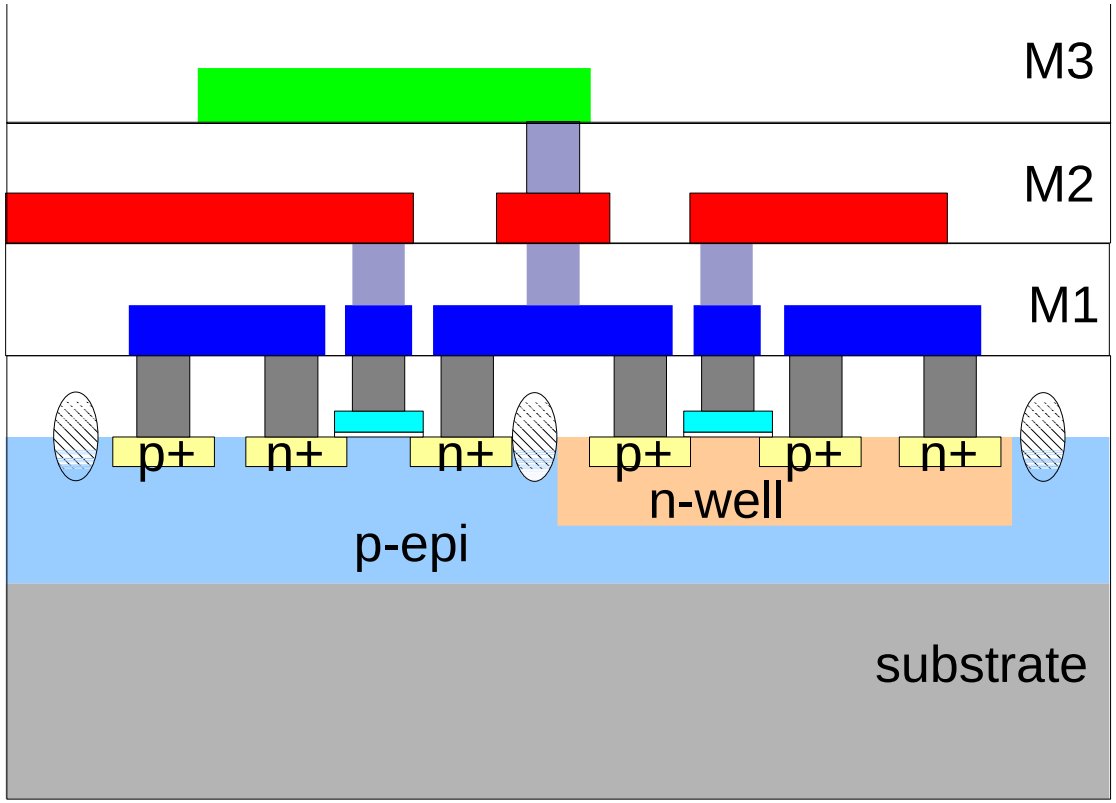


NAND2

Standard Cells (Layout)

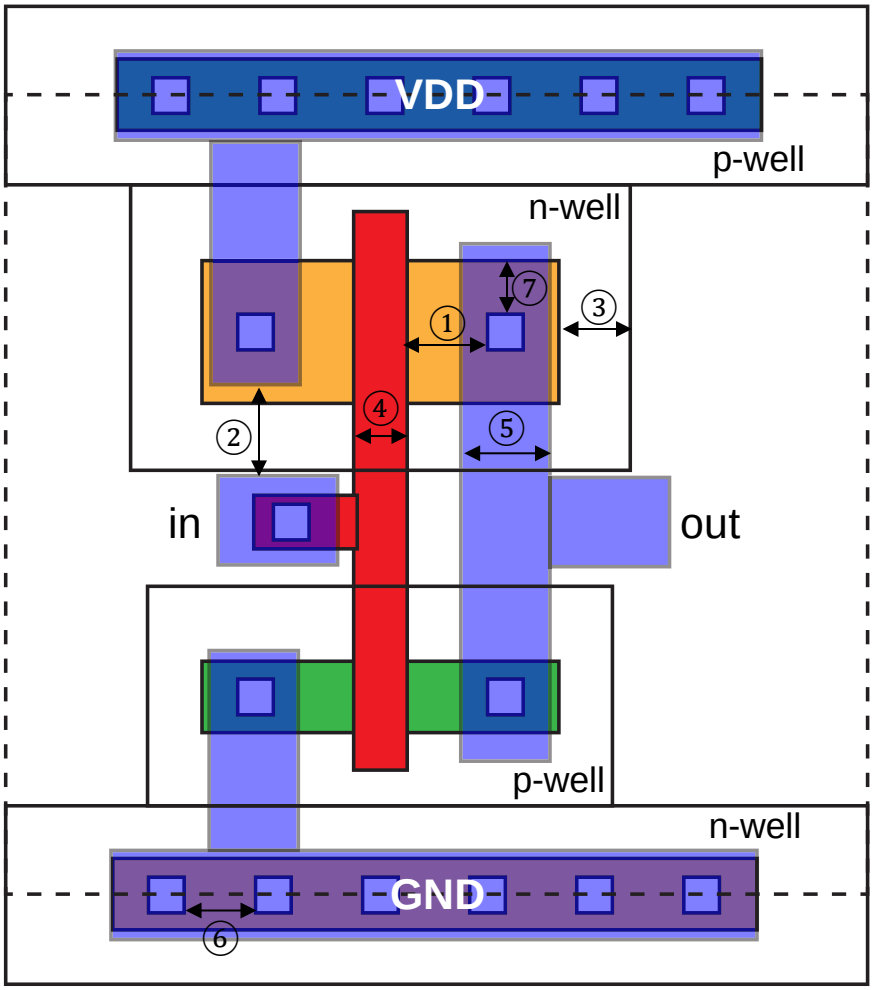


Top-down view



Side view

Design Rules



①: Min. distance (poly, contact)

②: Min. distance (metal 1)

③: Min. distance (p-active, n-well boundary)

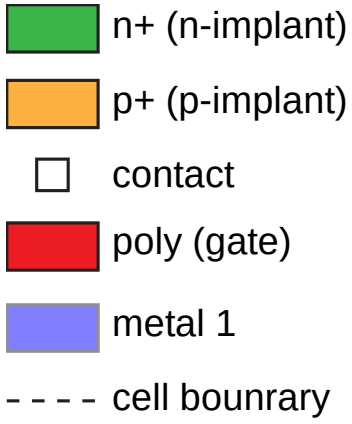
④: Min. width (poly)

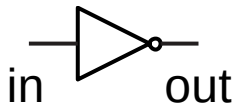
⑤: Min. width (metal 1)

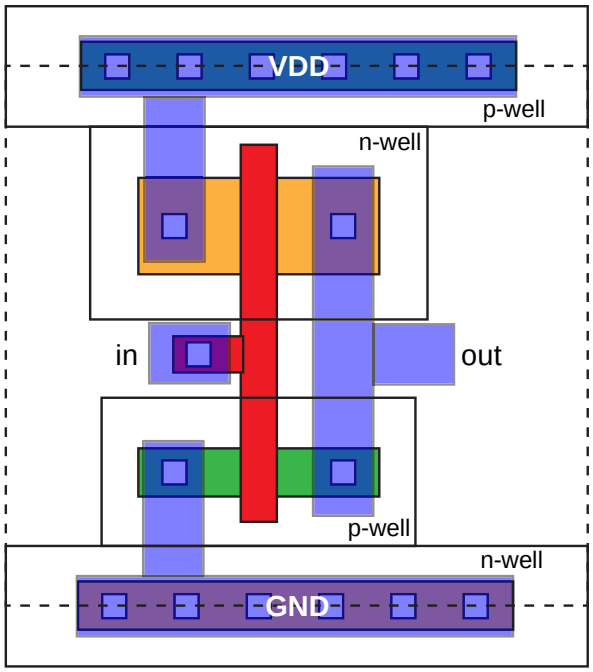
⑥: Min. distance (contact)

⑦: Min. distance (contact, n-well bounrary)

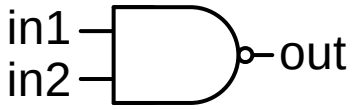
Standard Cells (Layout)

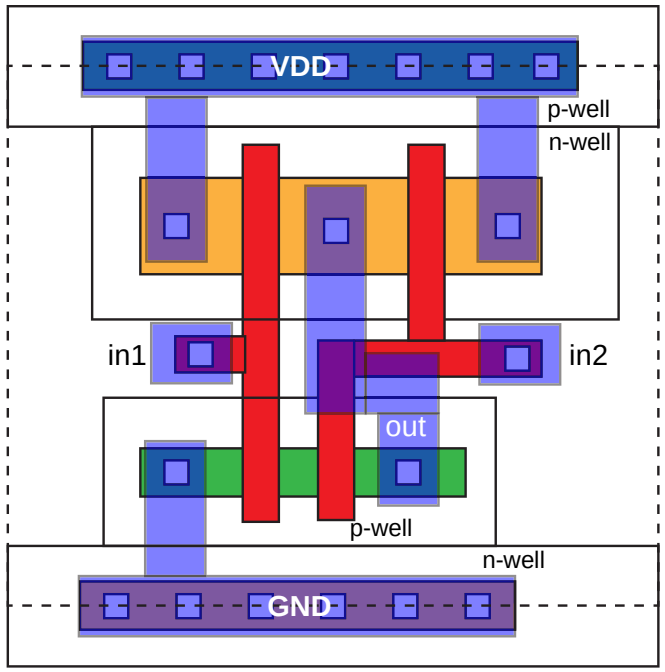






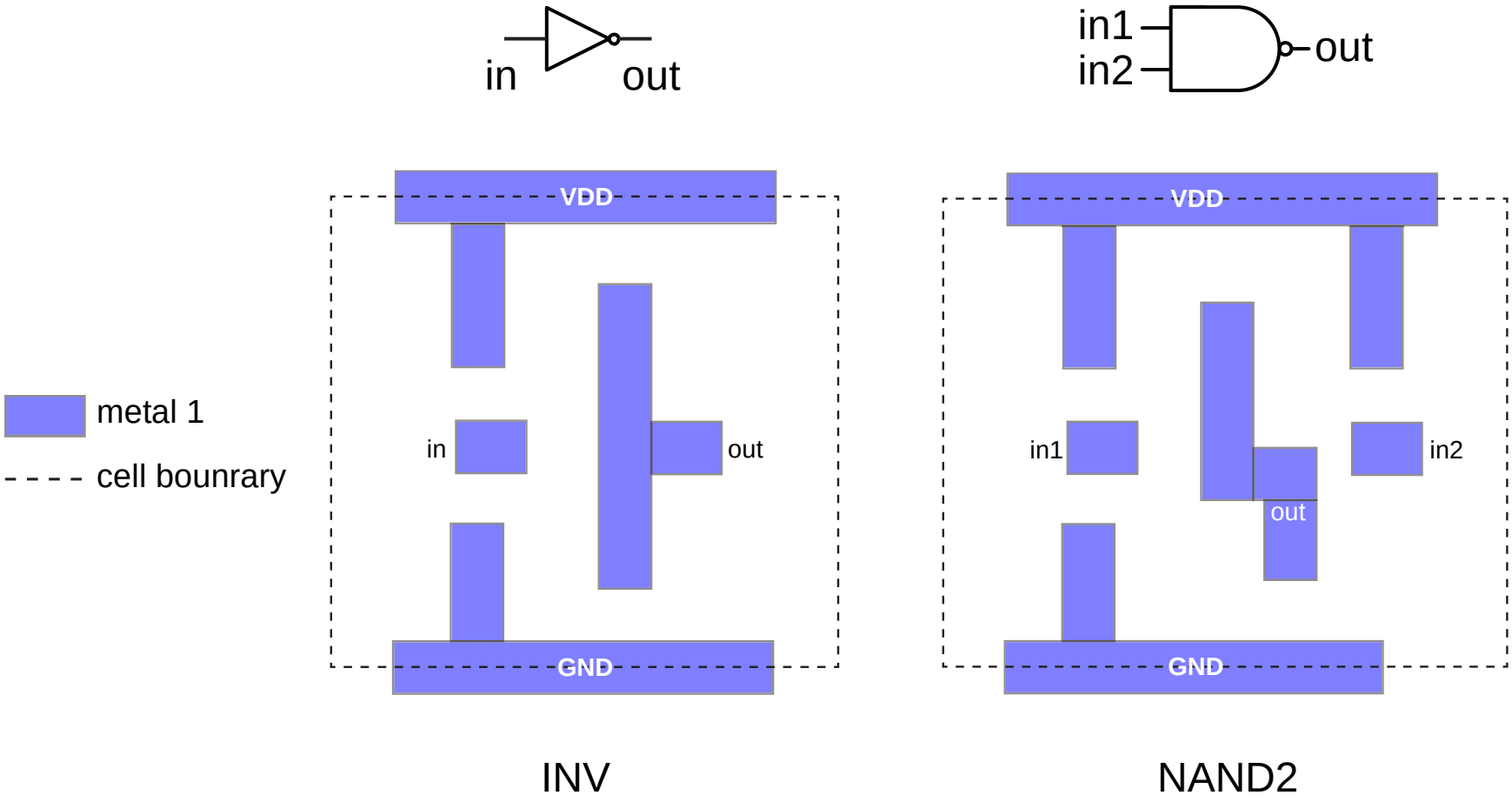
INV



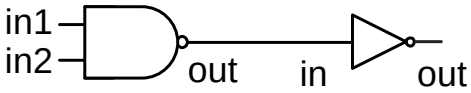


NAND2

Standard Cells (Abstract)



Standard-Cell-Based Design

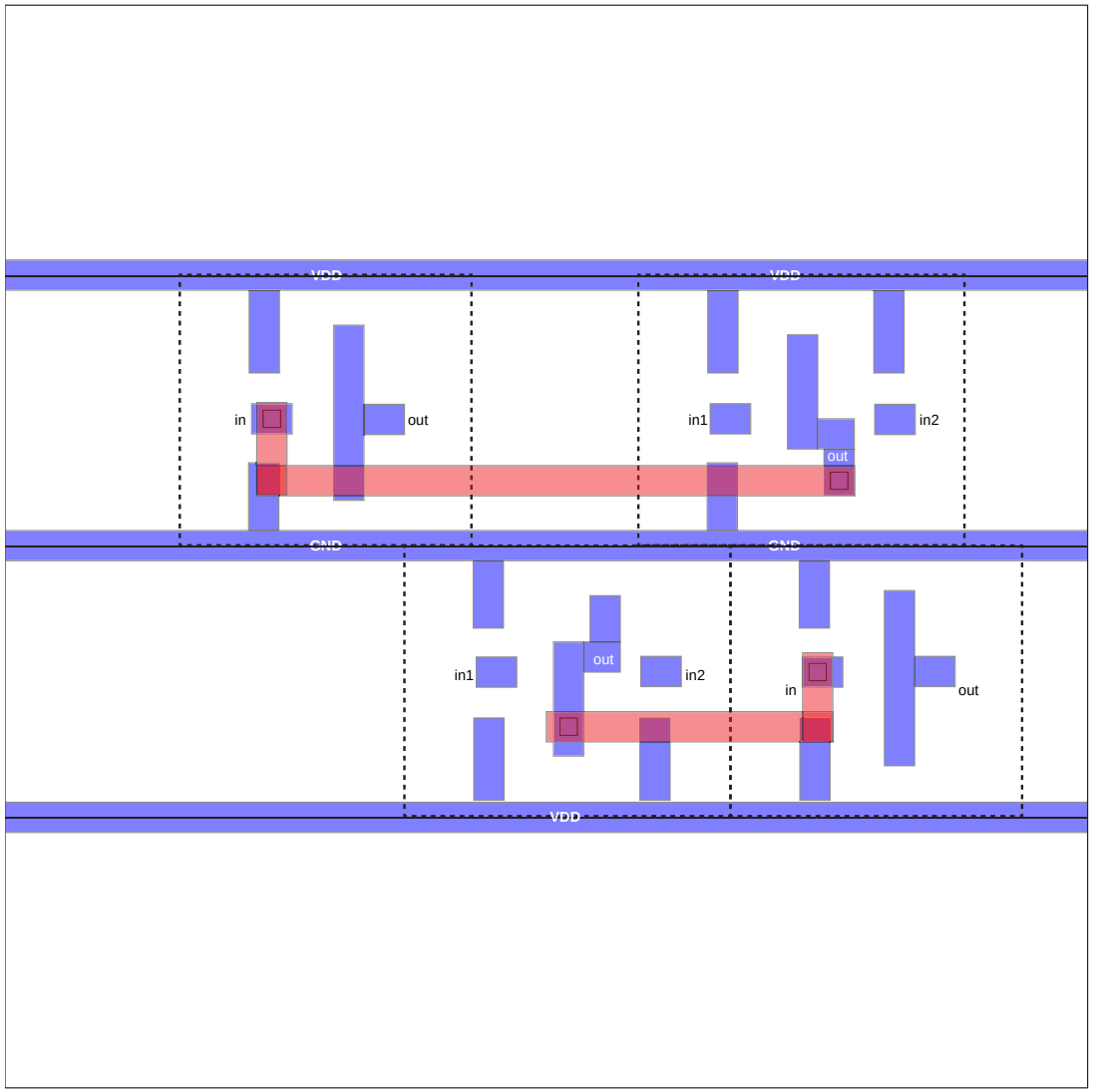


metal 1

cell bounrary

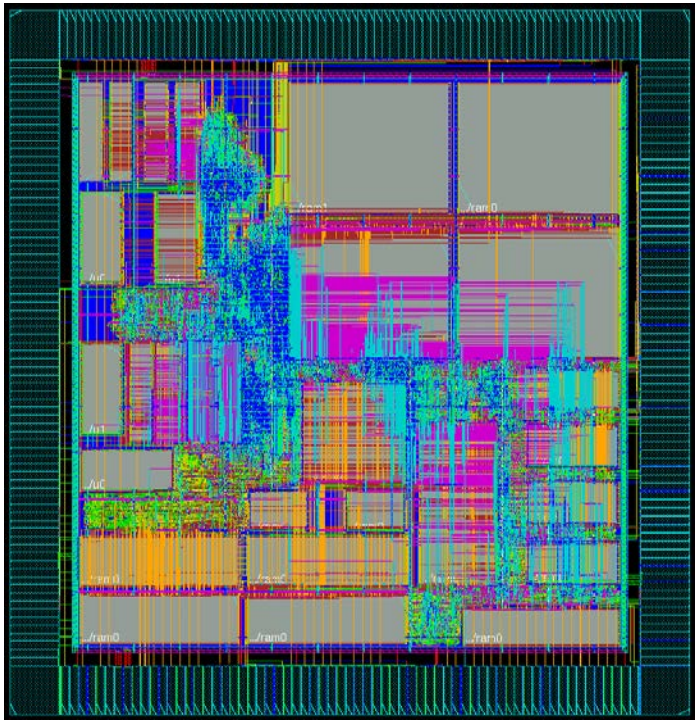
via12

metal 2



Standard-Cell-Based Design

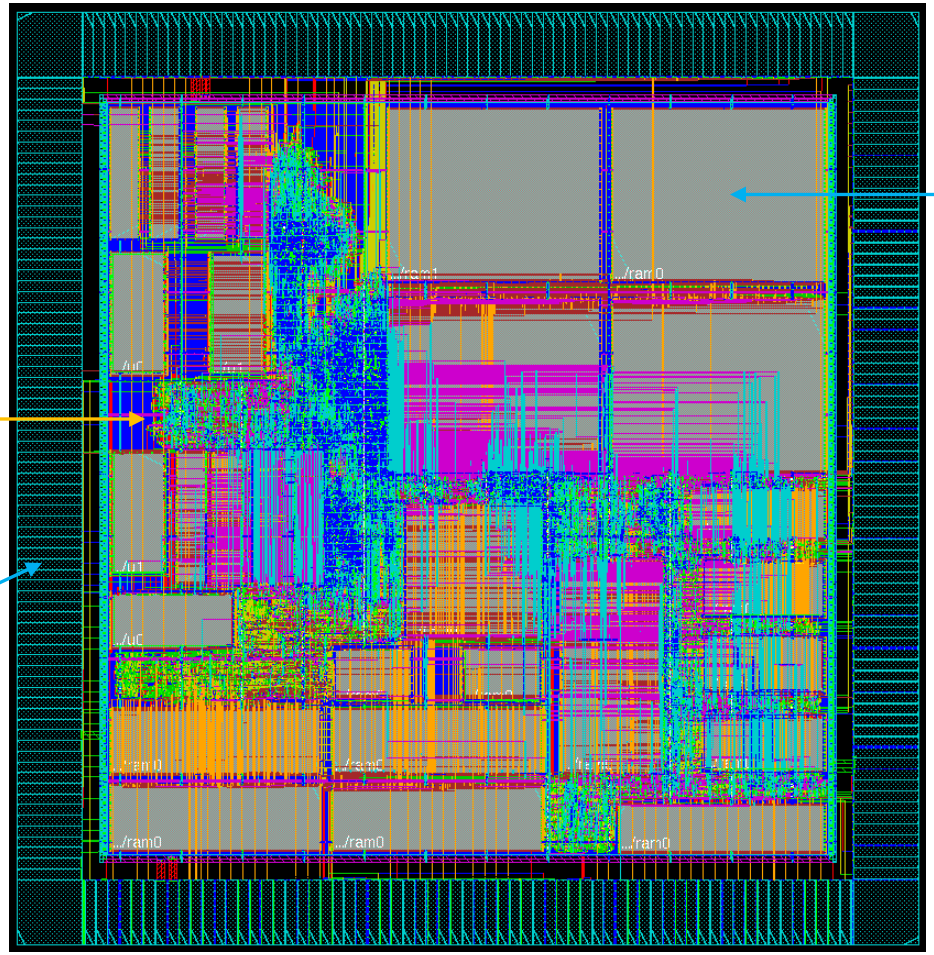
- Deal with
  - Standard cells (pre-drawn and pre-characterized)
  - Routing layers (M1, via12, M2, via23, …)



Standard-Cell-Based Design

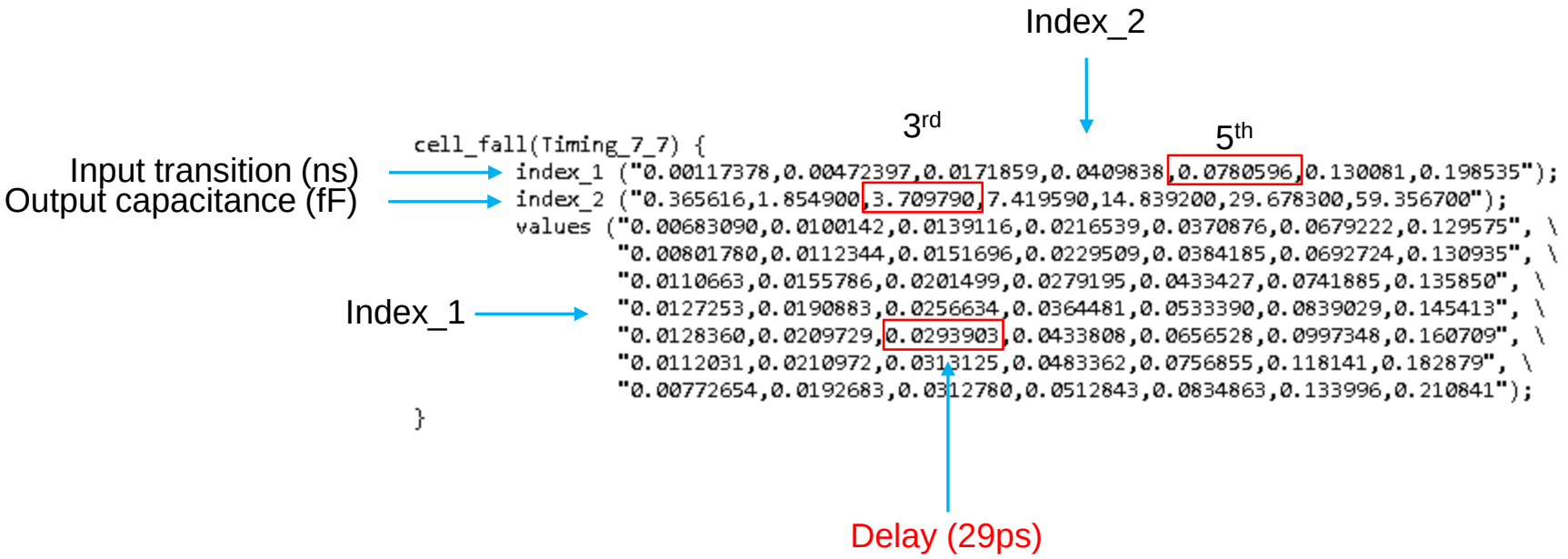
- Intellectual Property (IP) blocks
  - Pre-created blocks
    - Memory
    - Arithmetic
    - Cryptographic
    - DSP
    - Controller
    - …

Standard-Cell-Based Design



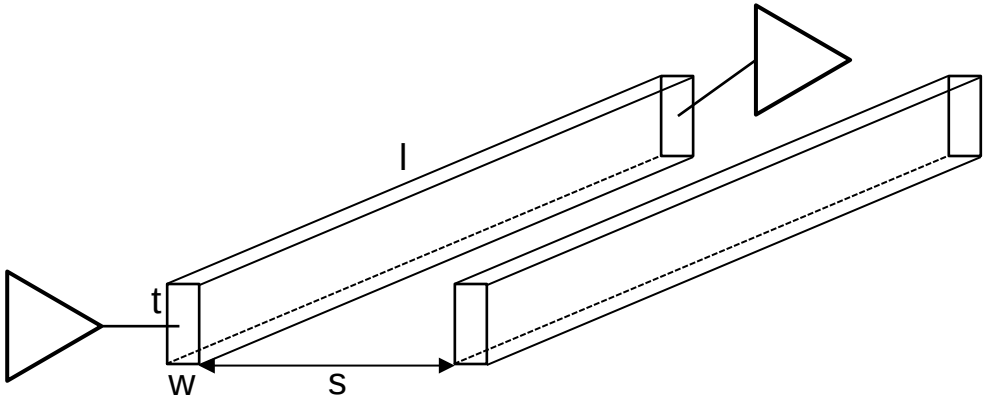
Delay Calculation & Timing Analysis

- Pre-characterized cells

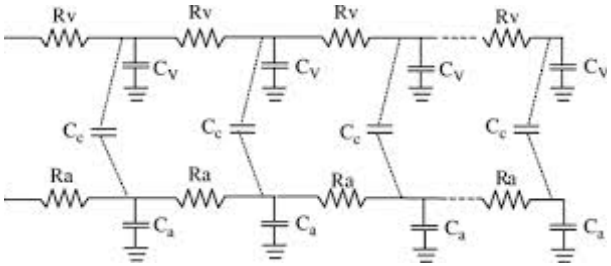


Delay Calculation

- Interconnect delay

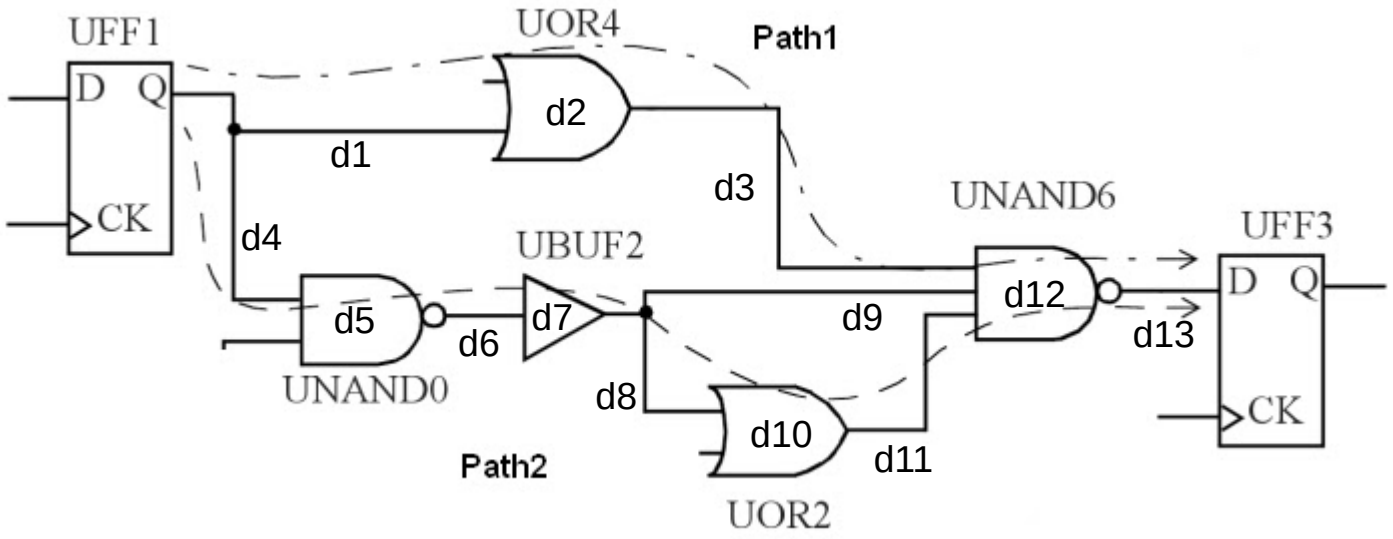


modeling



$$R = \rho \frac{l}{t \cdot w} \qquad C = \epsilon \frac{t \cdot l}{s} \qquad Delay \propto RC \propto l^2$$

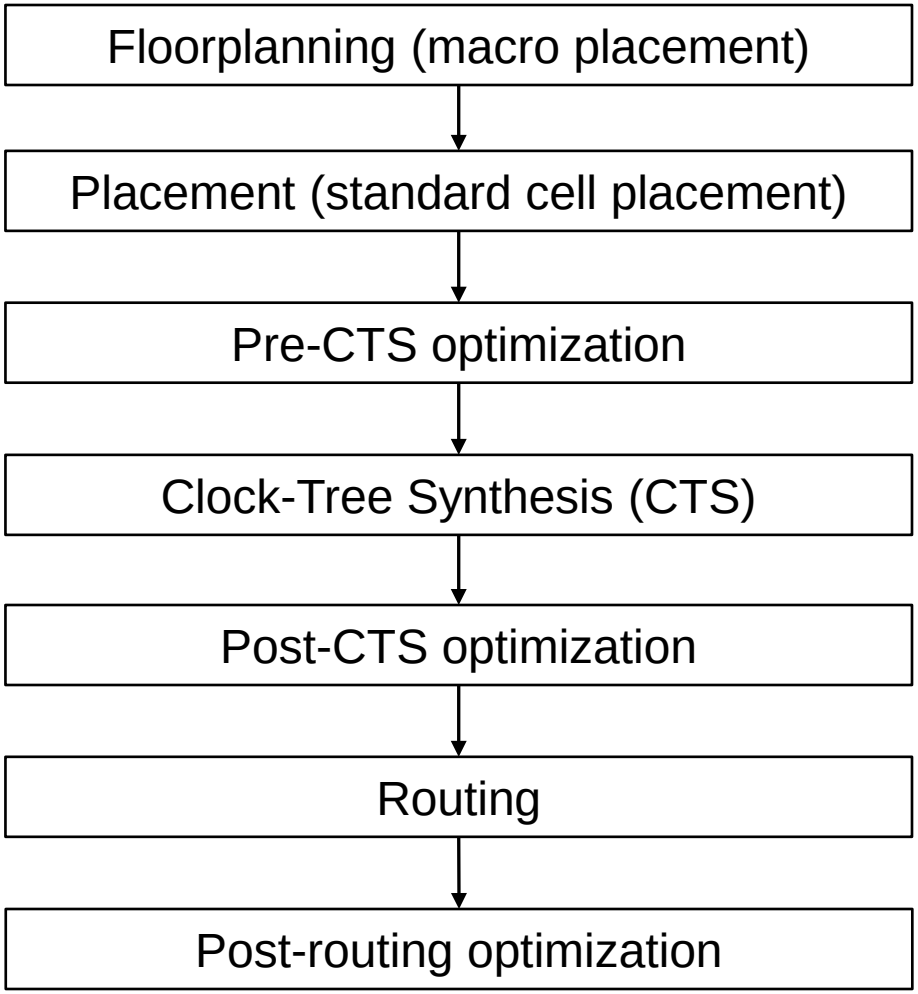
Timing Analysis



Standard-Cell-Based Design

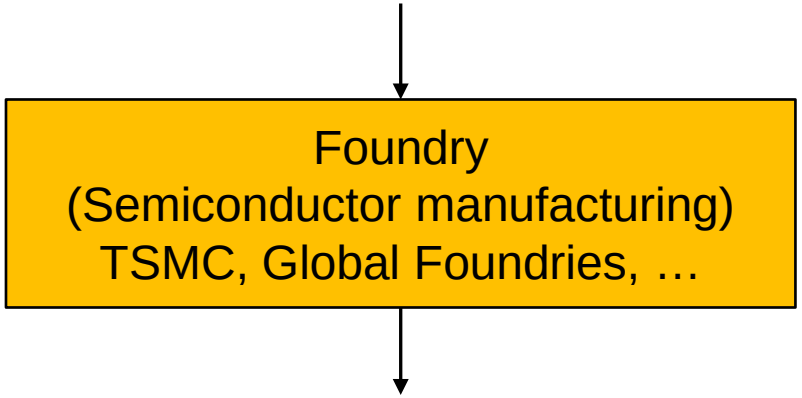
- What should we do?
  - Find the locations of the macros.
  - Find the locations of the standard cells.
  - Route the macros and the standard cells.
    - Power/ground
    - Signal
    - Clock
    - Bus
  - Extract parasitic RC.
  - Analyze the final layout.
    - Timing (clock frequency)
    - Power consumption (dynamic / leakage)
    - Area
    - Power integrity
    - Signal integrity
    - Thermal

Standard-Cell-Based Design

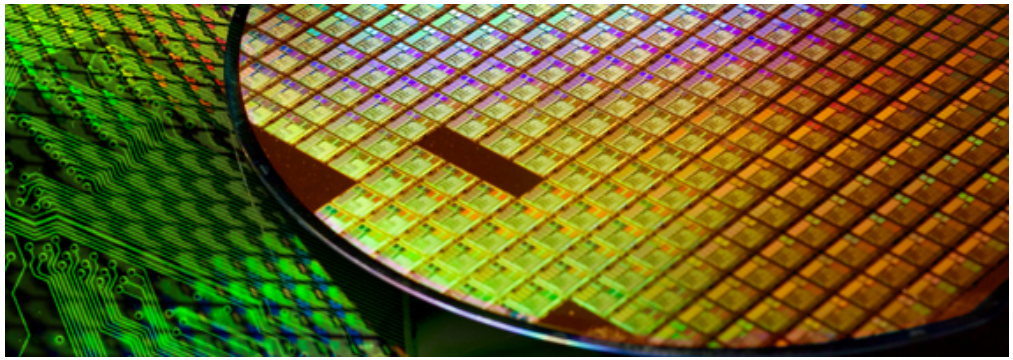


Semiconductor Manufacturing

Layout (GDSII stream format)

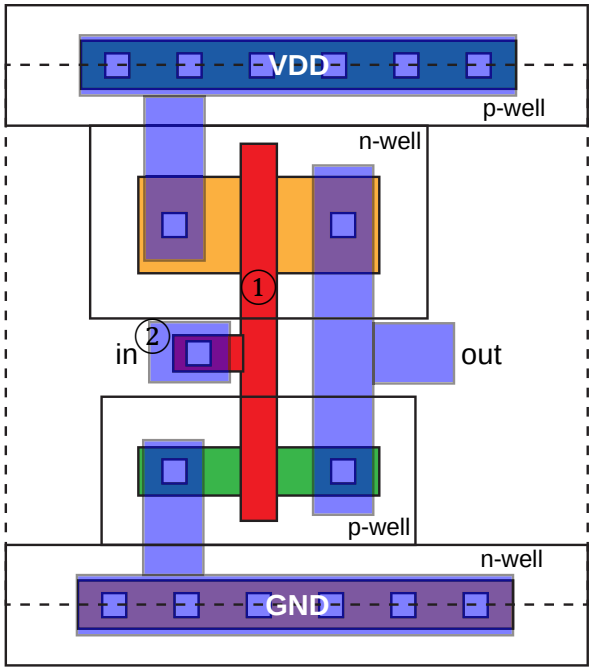


Bare dies



Semiconductor Manufacturing

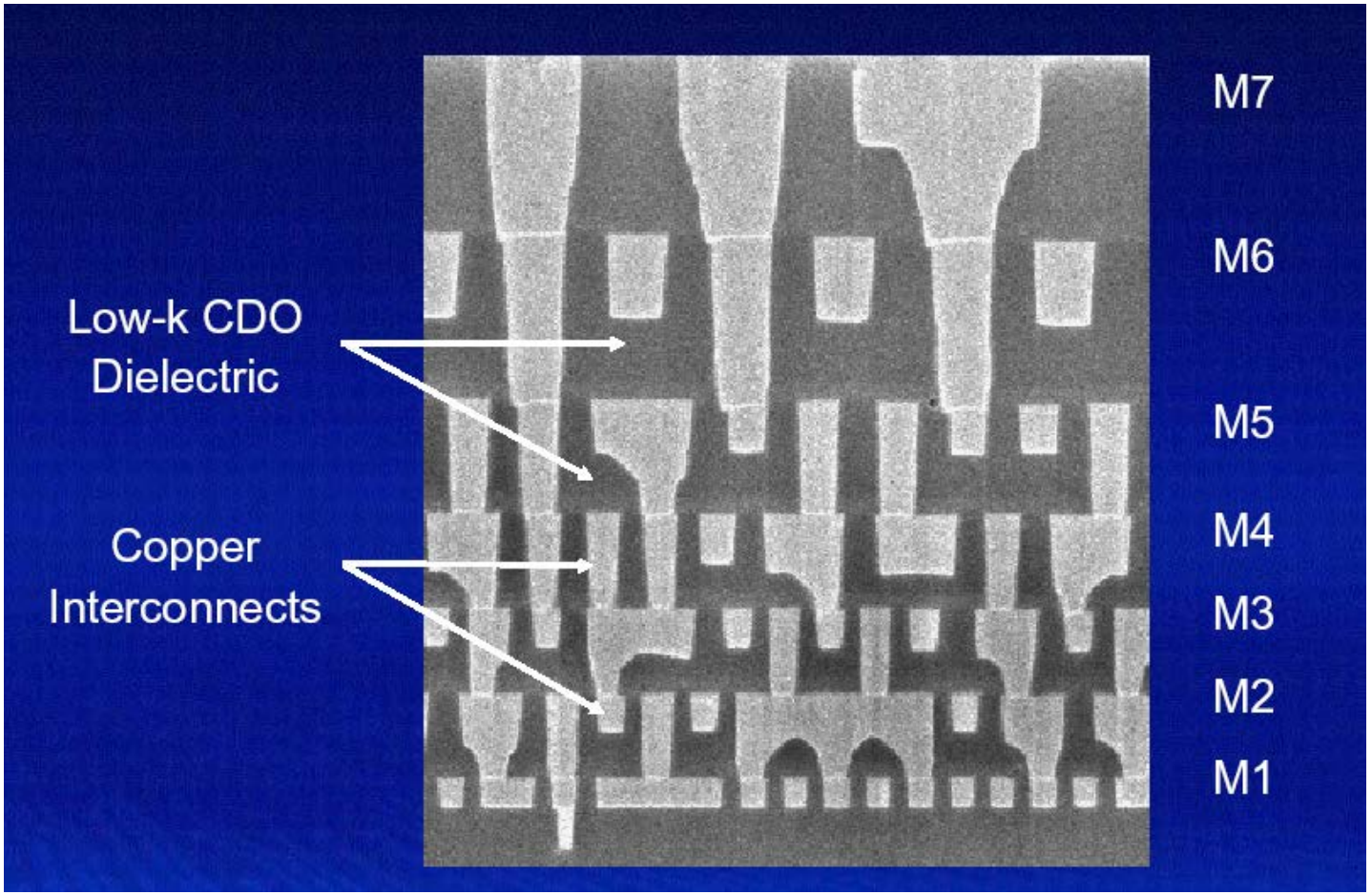
- Input
  - Layout (GDSII stream format)
    - A set of geometric objects



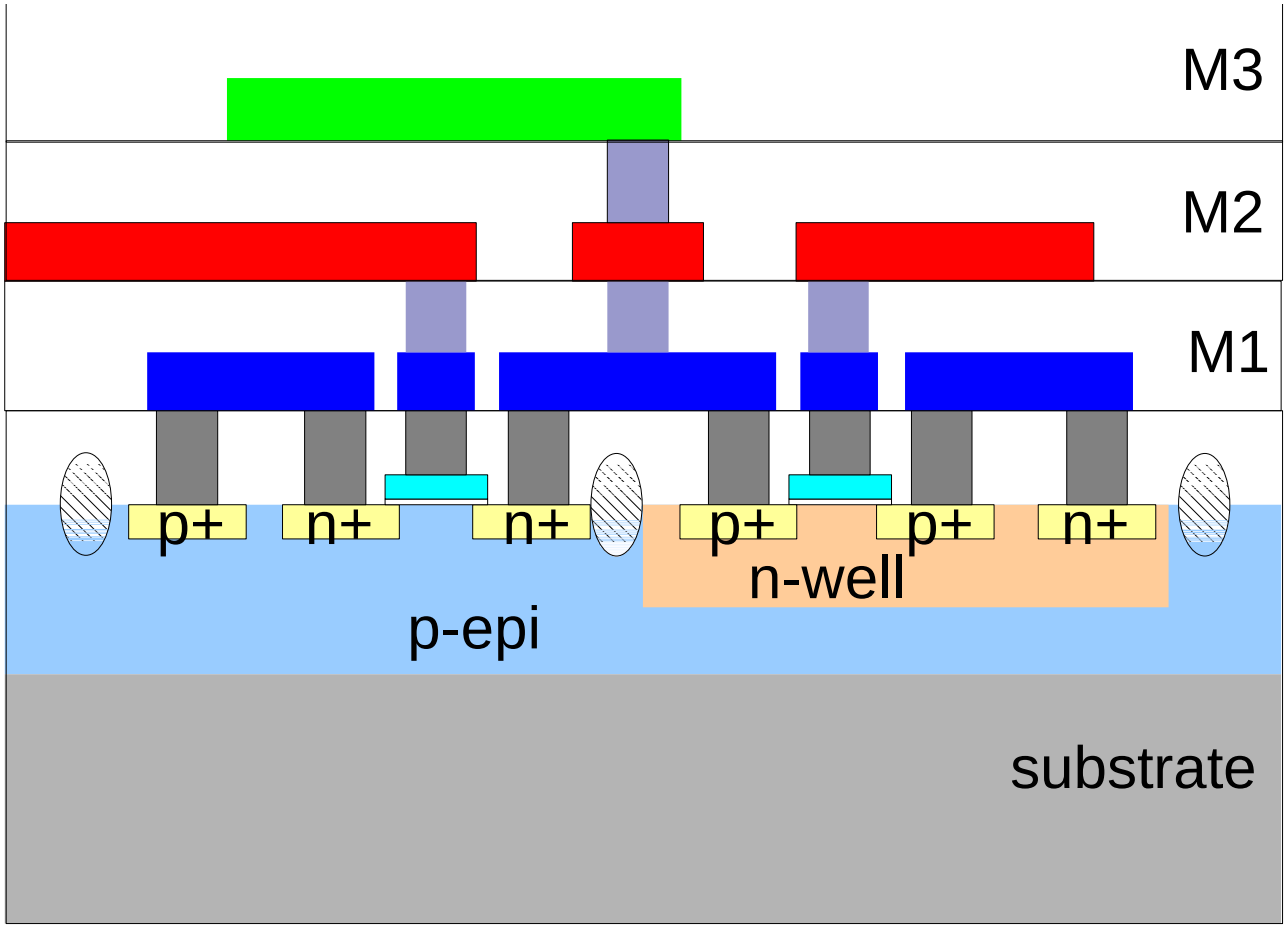
①: Layer id 3, polygon { 50, 40, 70, 40, 70, 220, 50, 220, 50, 140, 20, 140, 20, 110, 50, 110, 50, 40 }

②: Layer id 7, rectangle { 10, 105, 40, 150 }

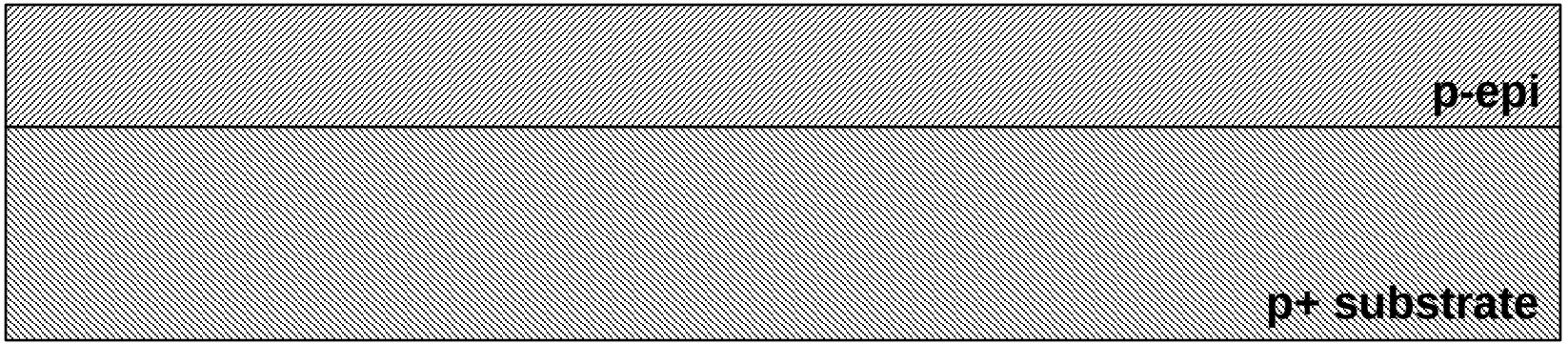
Semiconductor Manufacturing



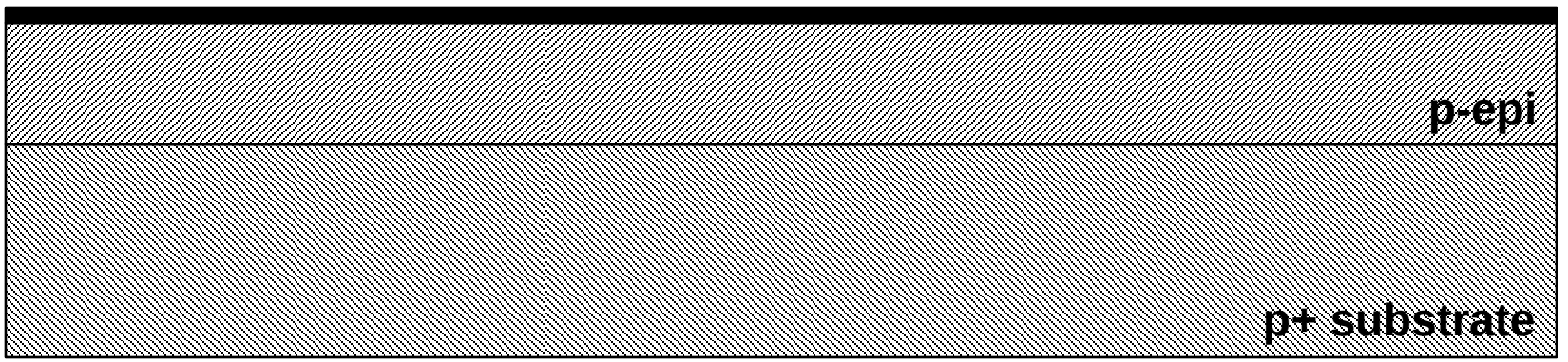
Semiconductor Manufacturing



Semiconductor Manufacturing

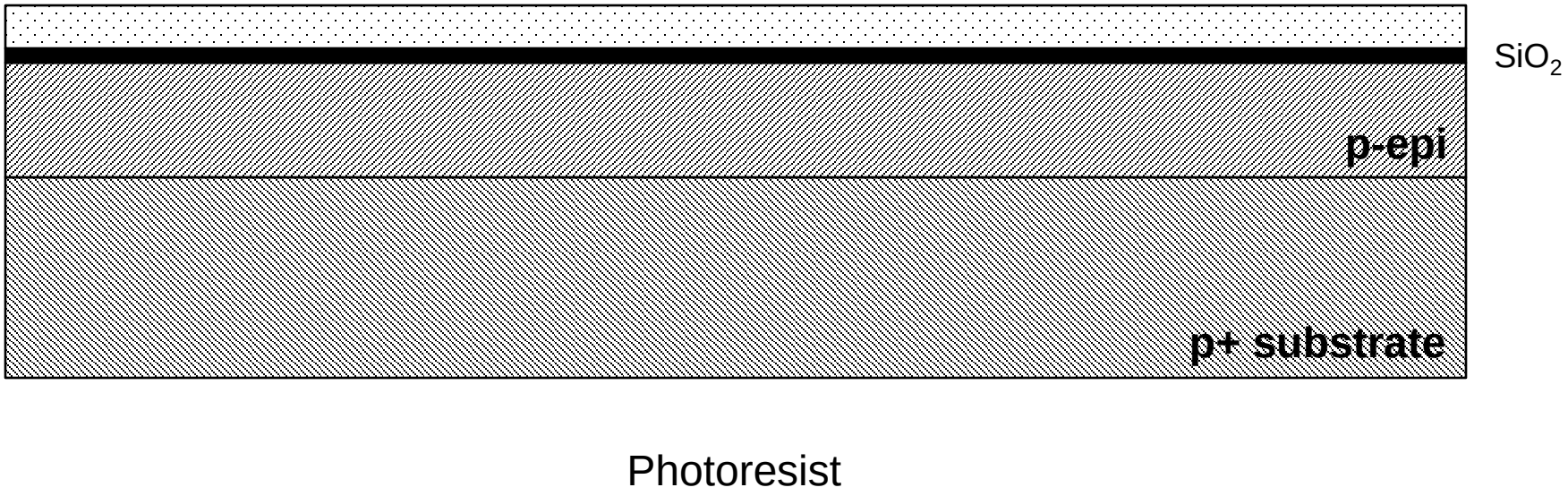


Semiconductor Manufacturing

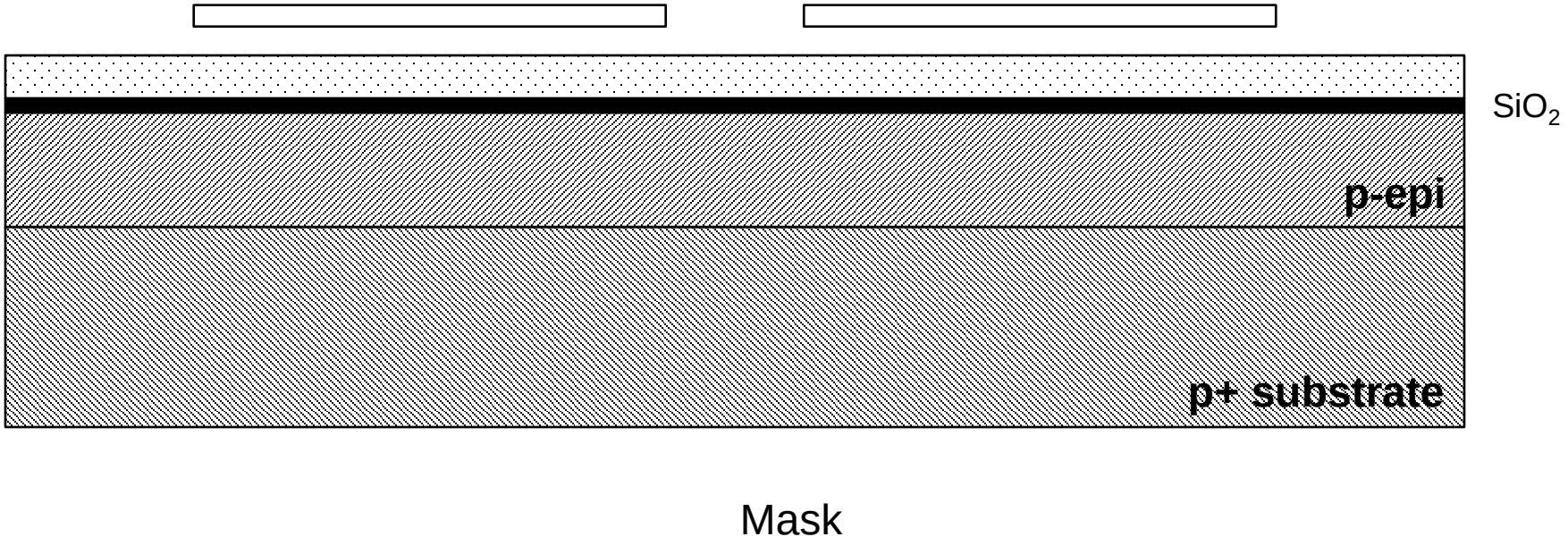


Gate-oxide deposition

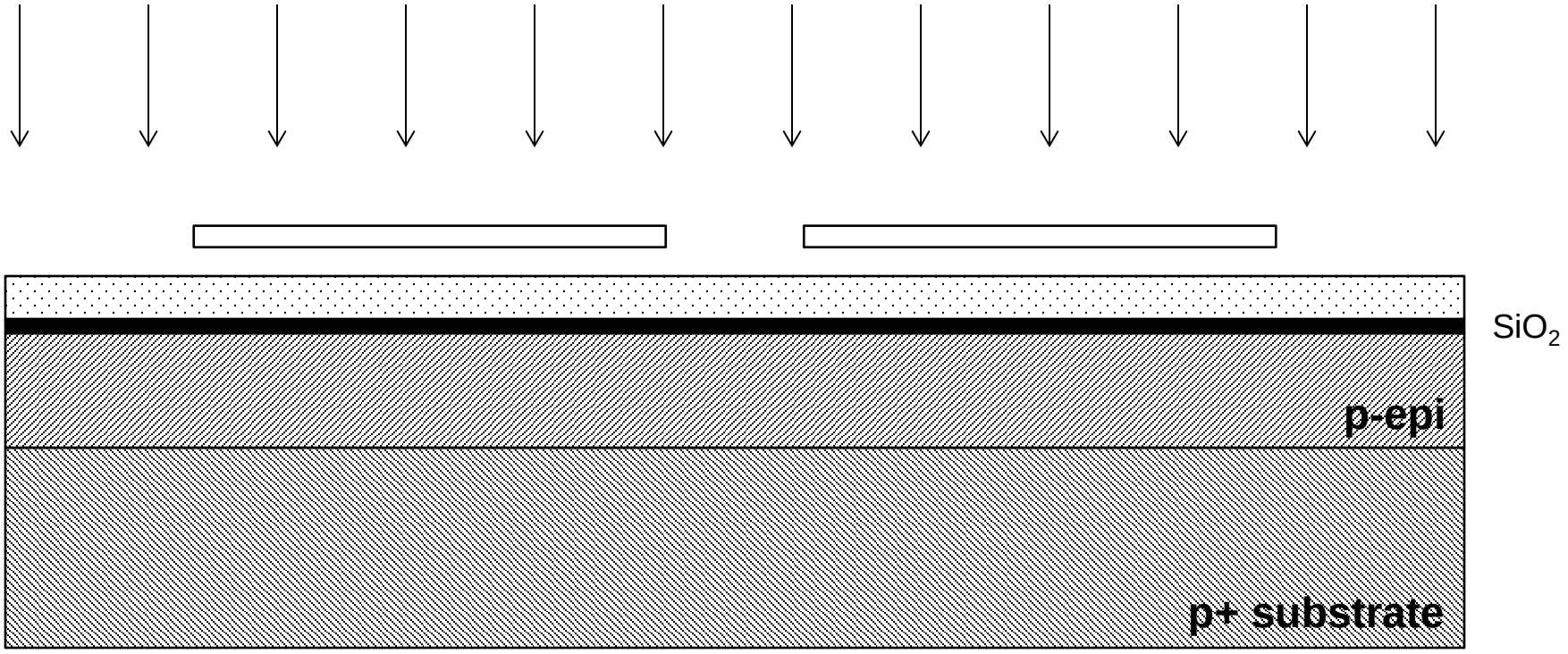
Semiconductor Manufacturing



Semiconductor Manufacturing

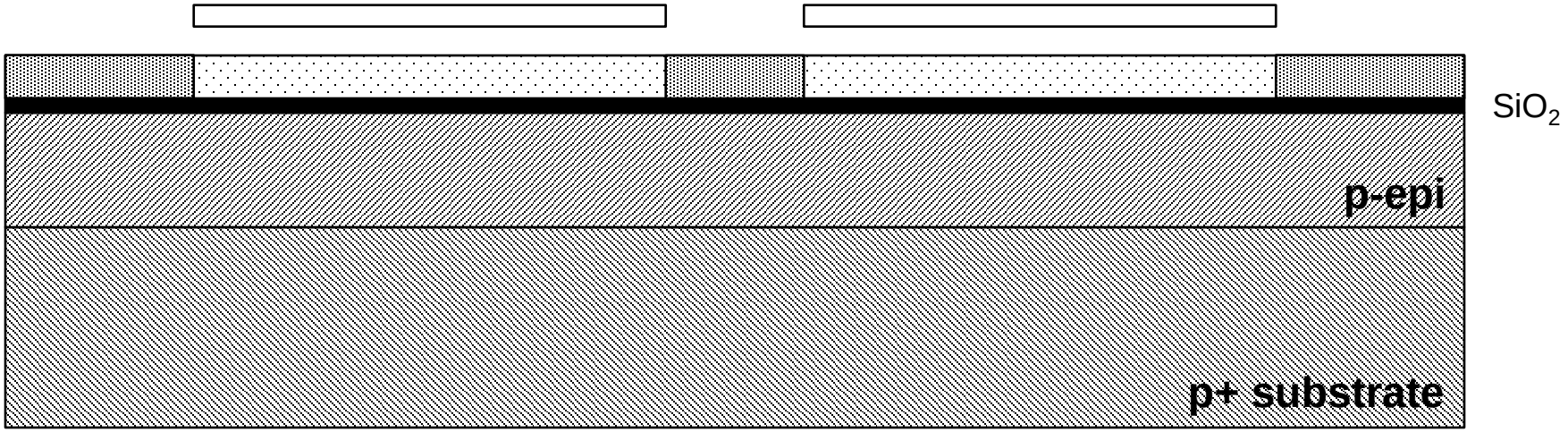


Semiconductor Manufacturing



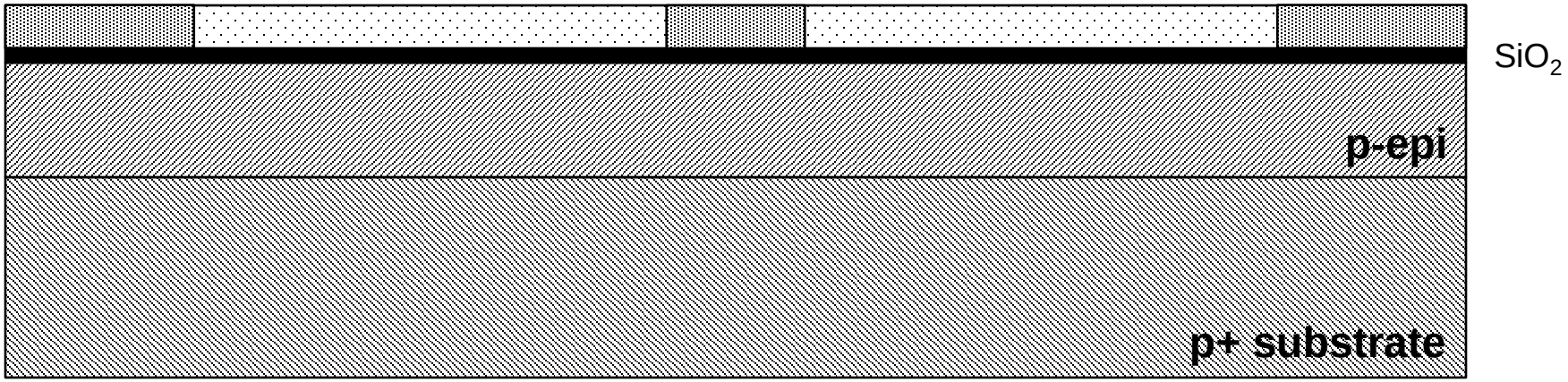
Expose (photolithography)

Semiconductor Manufacturing



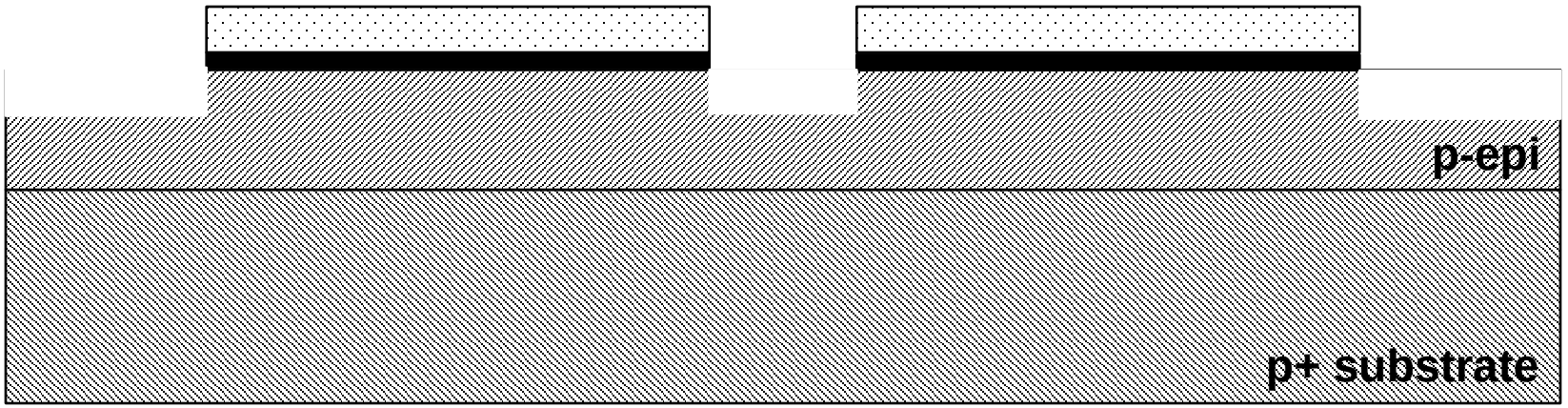
After photolithography

Semiconductor Manufacturing



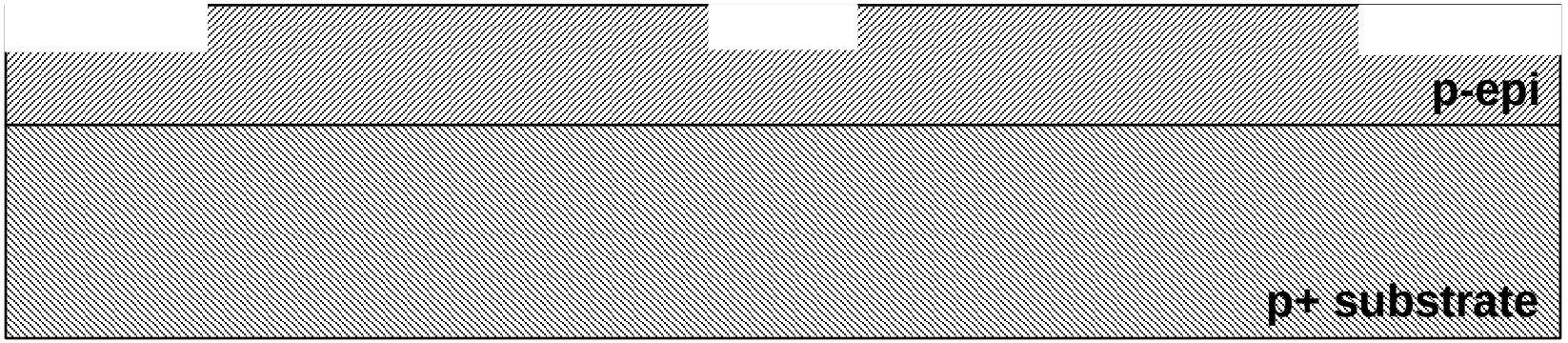
Remove mask

Semiconductor Manufacturing



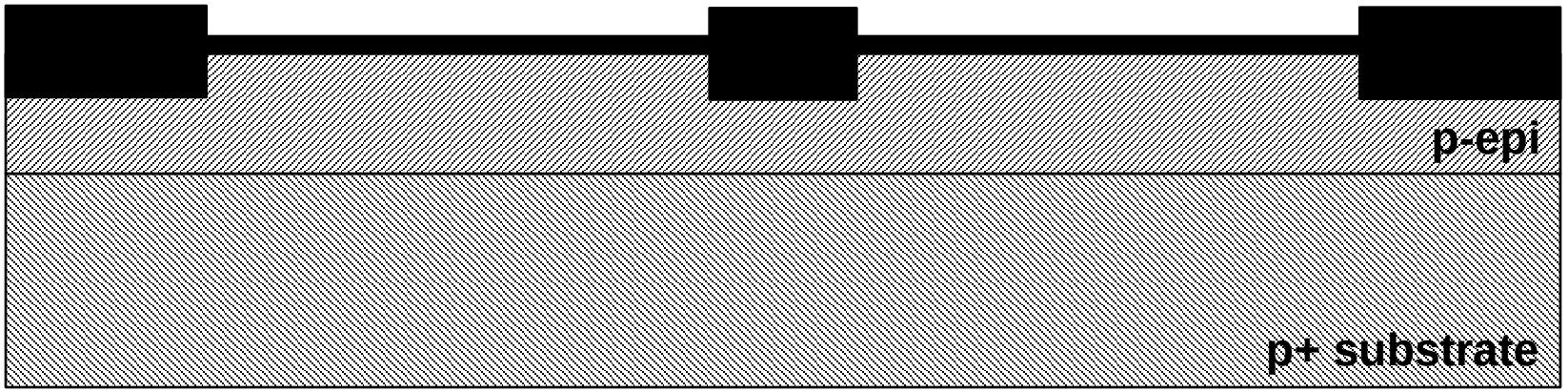
Etching

Semiconductor Manufacturing



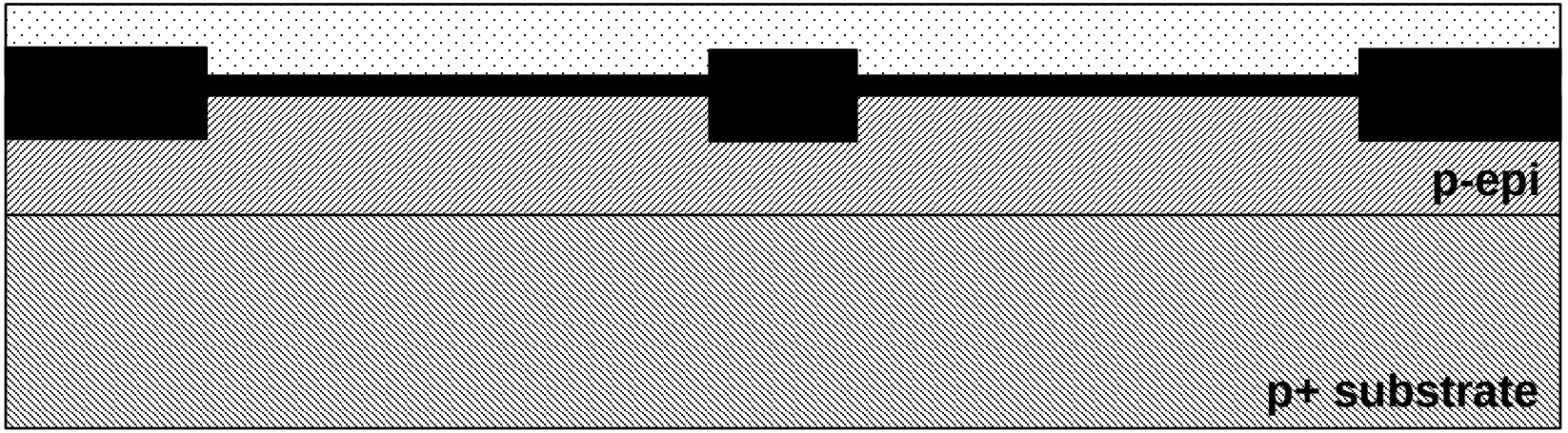
Etching

Semiconductor Manufacturing



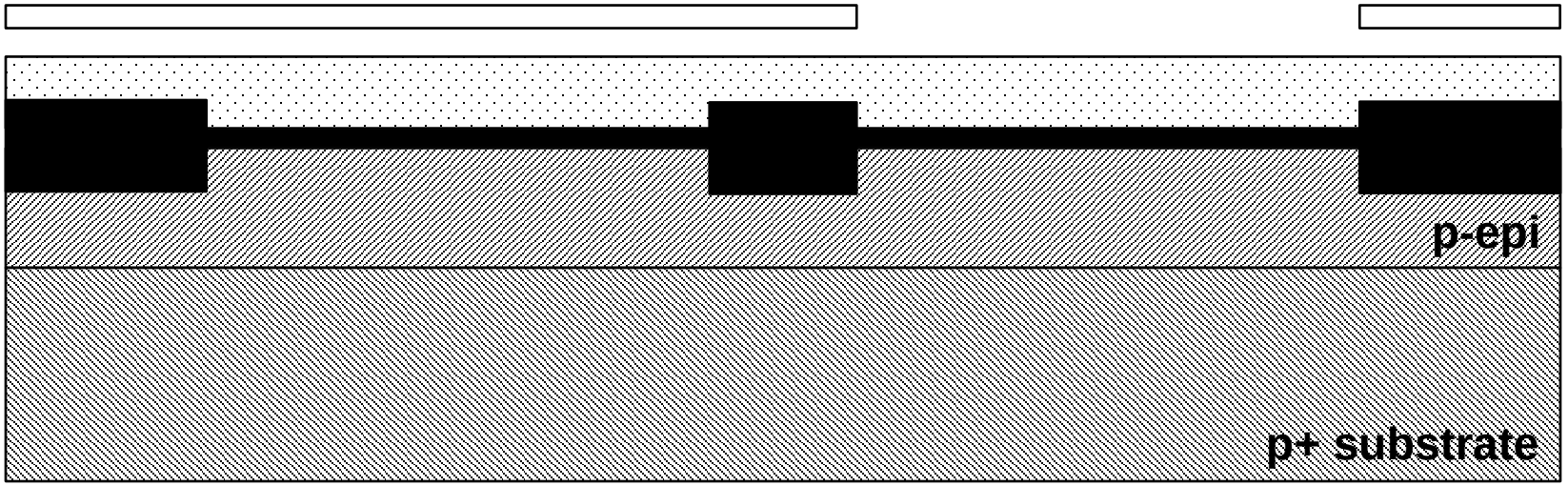
Oxide deposition

Semiconductor Manufacturing



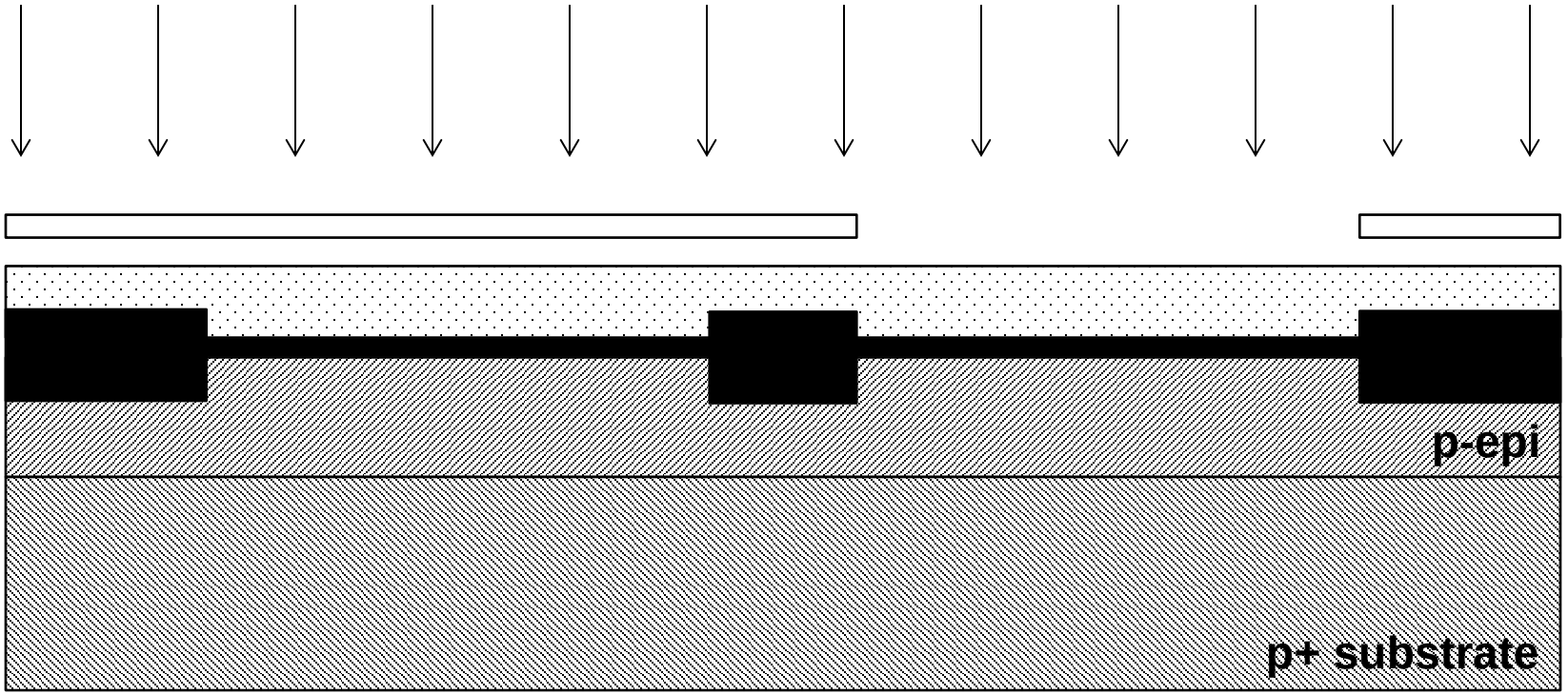
Photoresist

Semiconductor Manufacturing



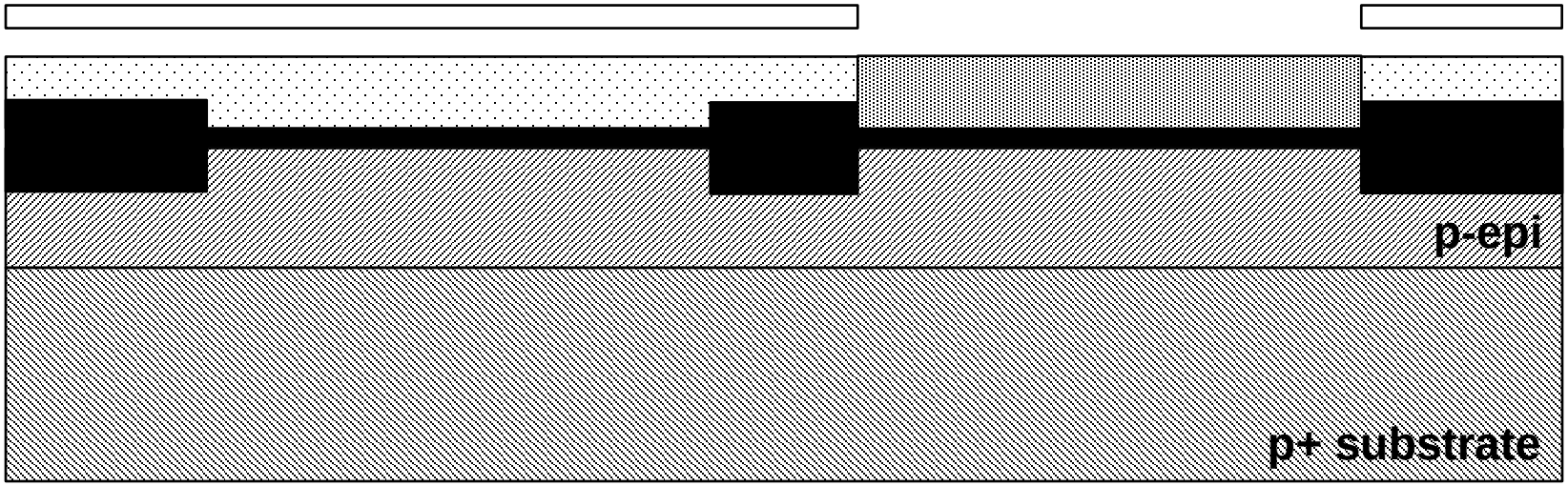
Mask

Semiconductor Manufacturing



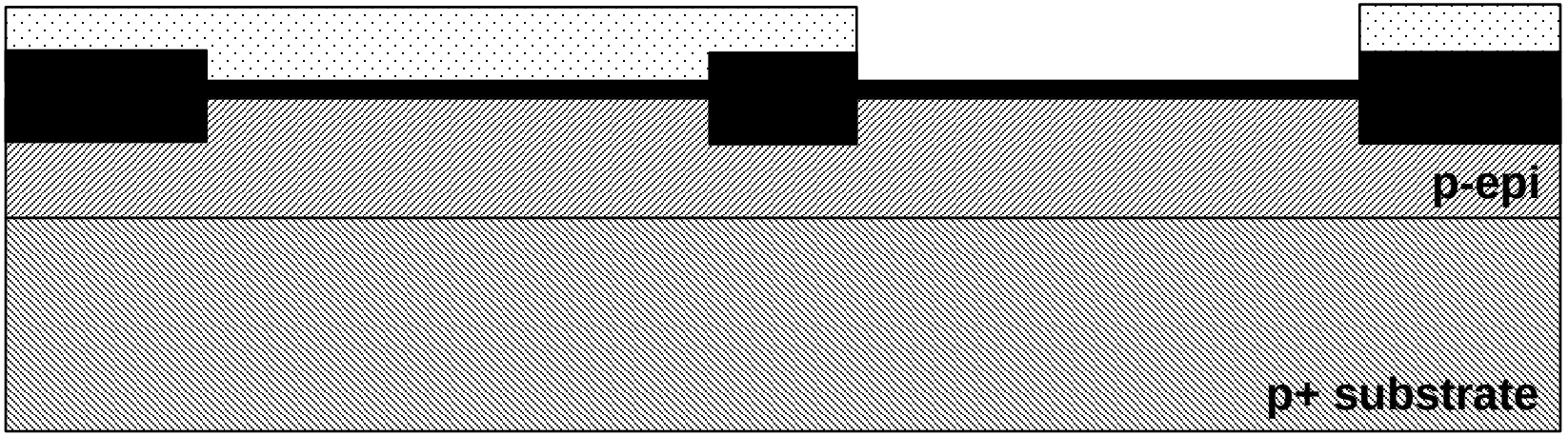
Photolithography

Semiconductor Manufacturing



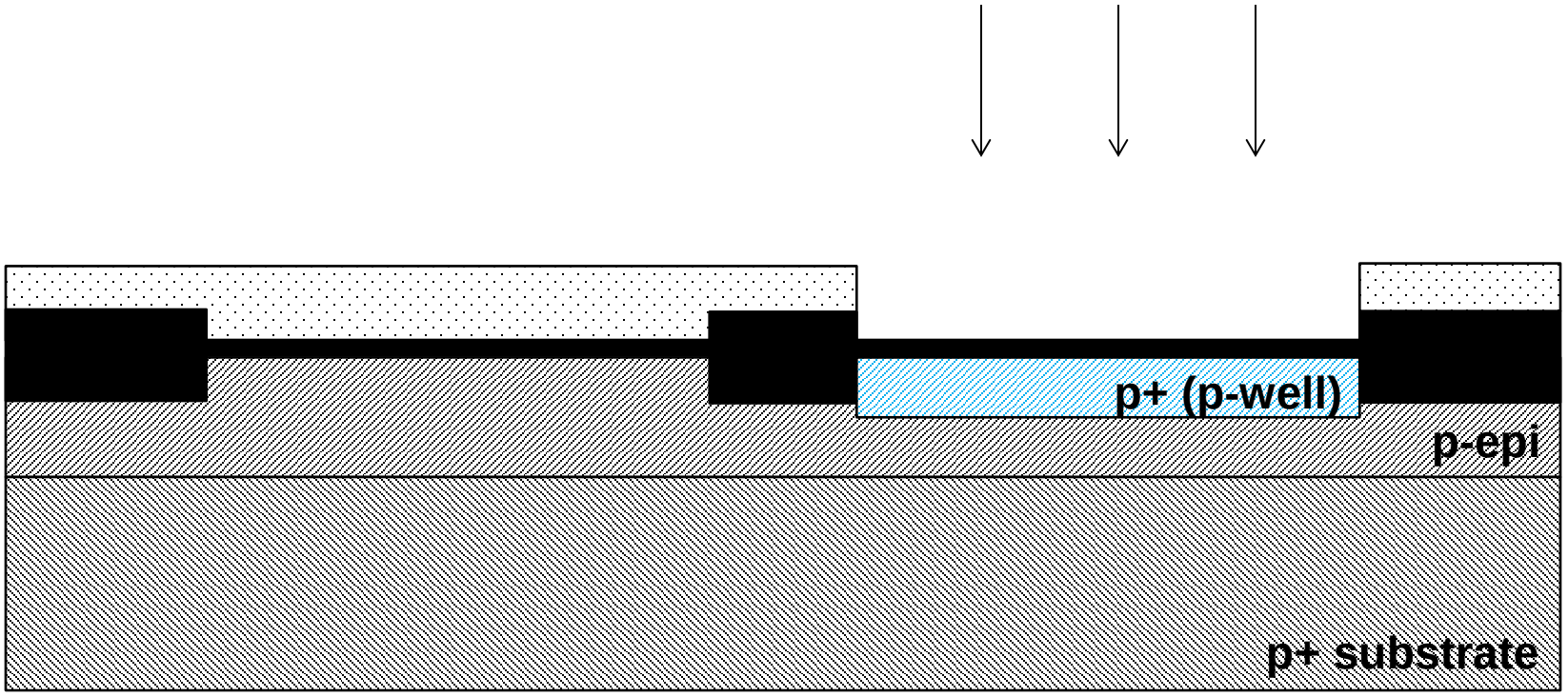
After photolithography

Semiconductor Manufacturing



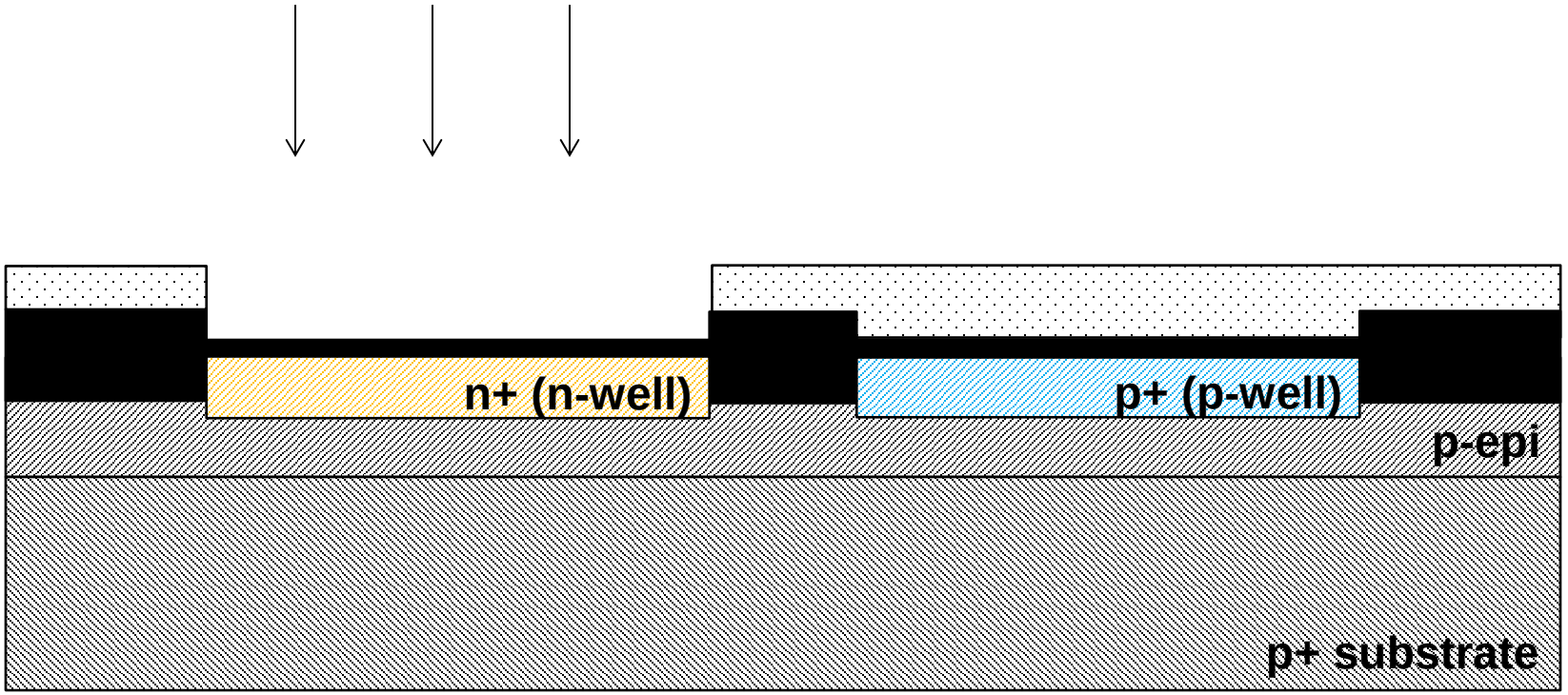
Etch

Semiconductor Manufacturing



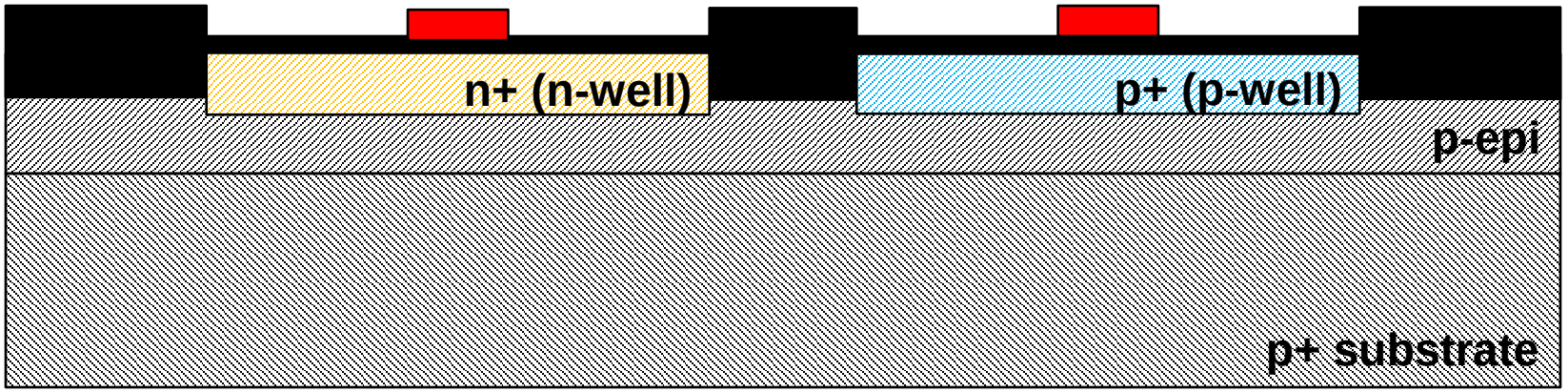
Doping

Semiconductor Manufacturing



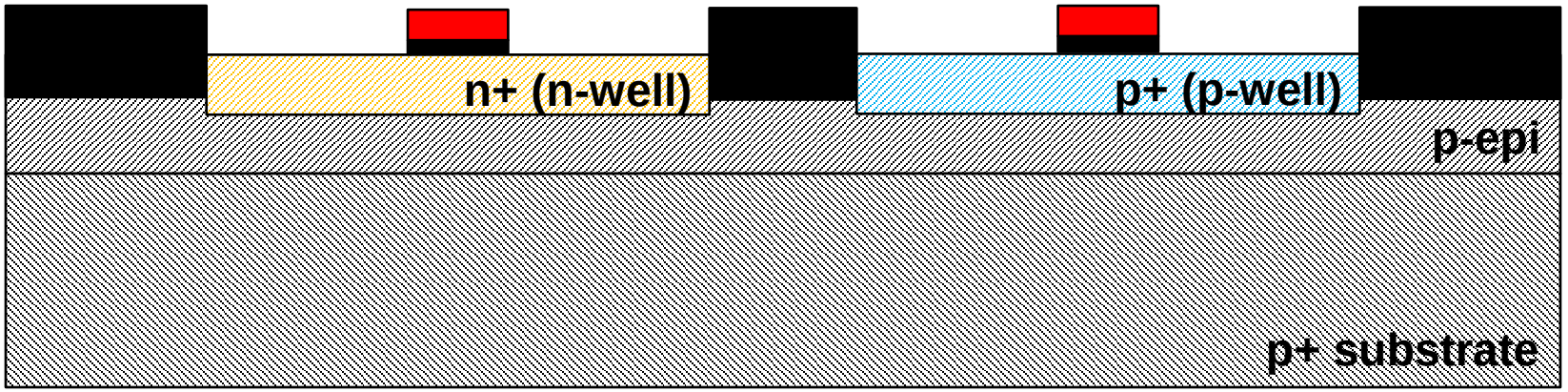
Doping

Semiconductor Manufacturing



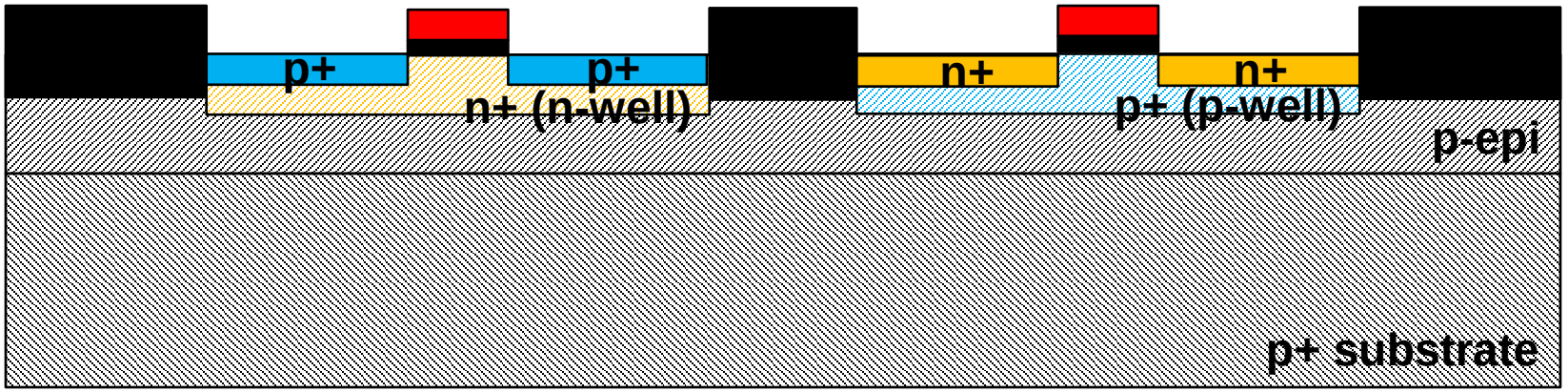
Poly

Semiconductor Manufacturing



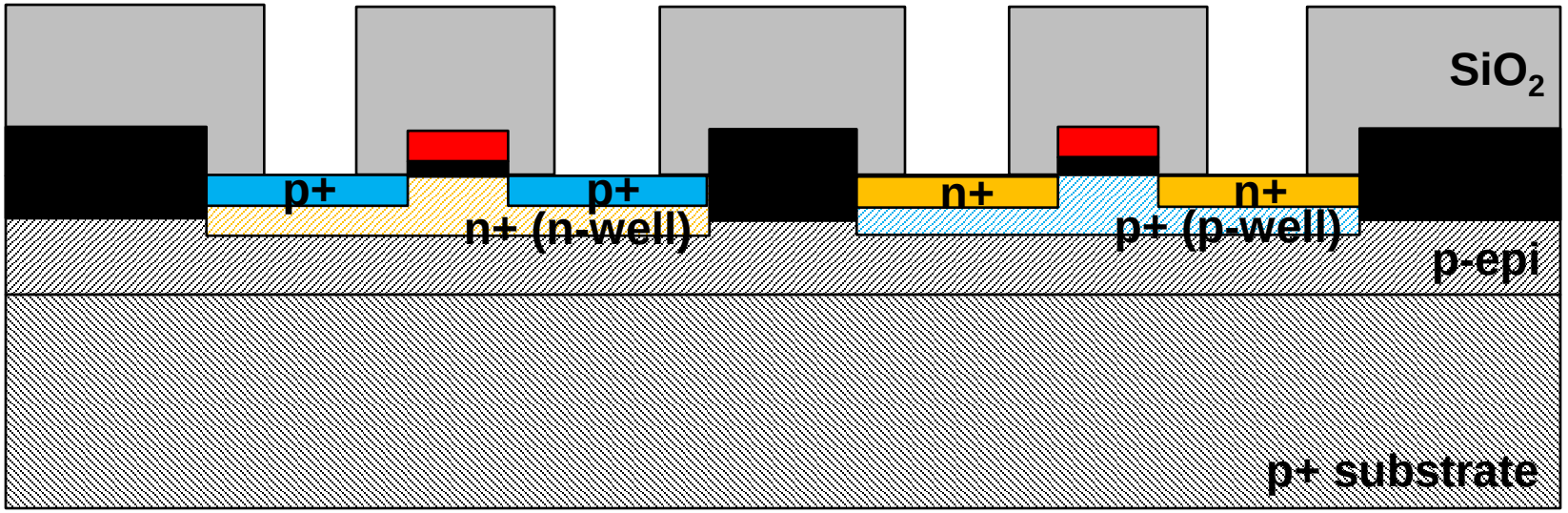
Etch

Semiconductor Manufacturing



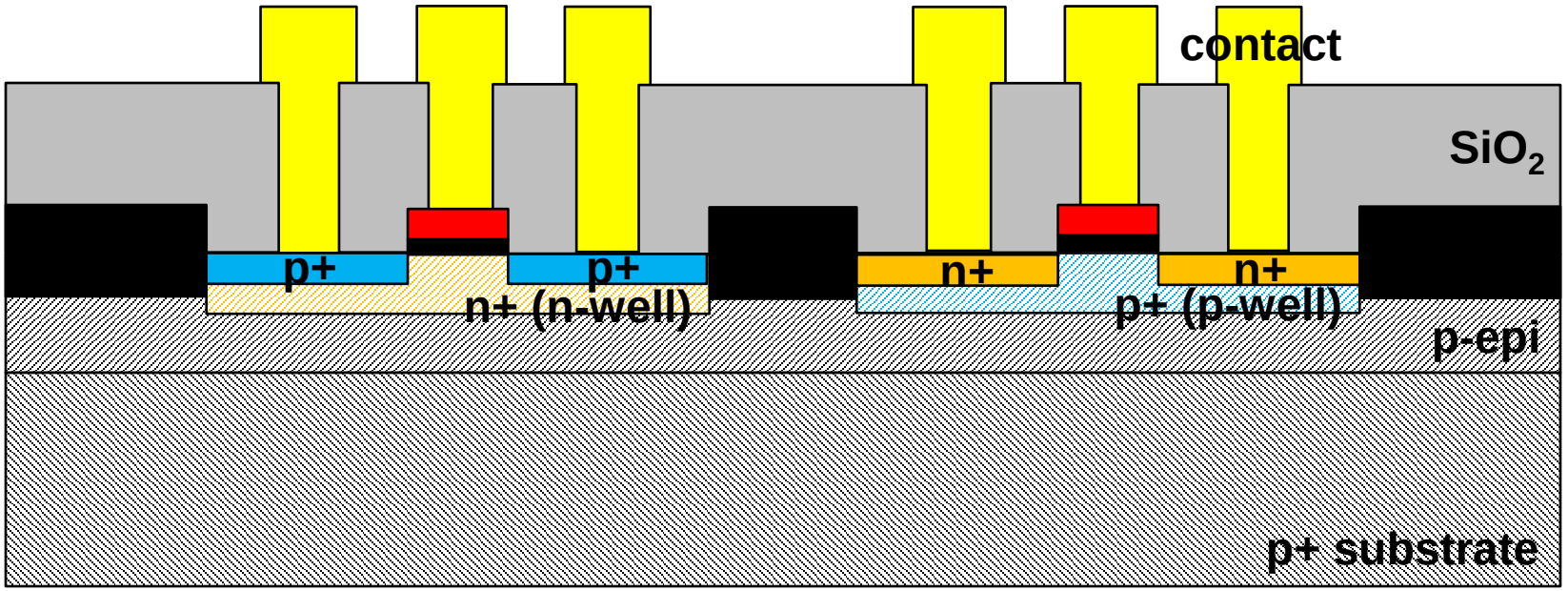
Doping

Semiconductor Manufacturing



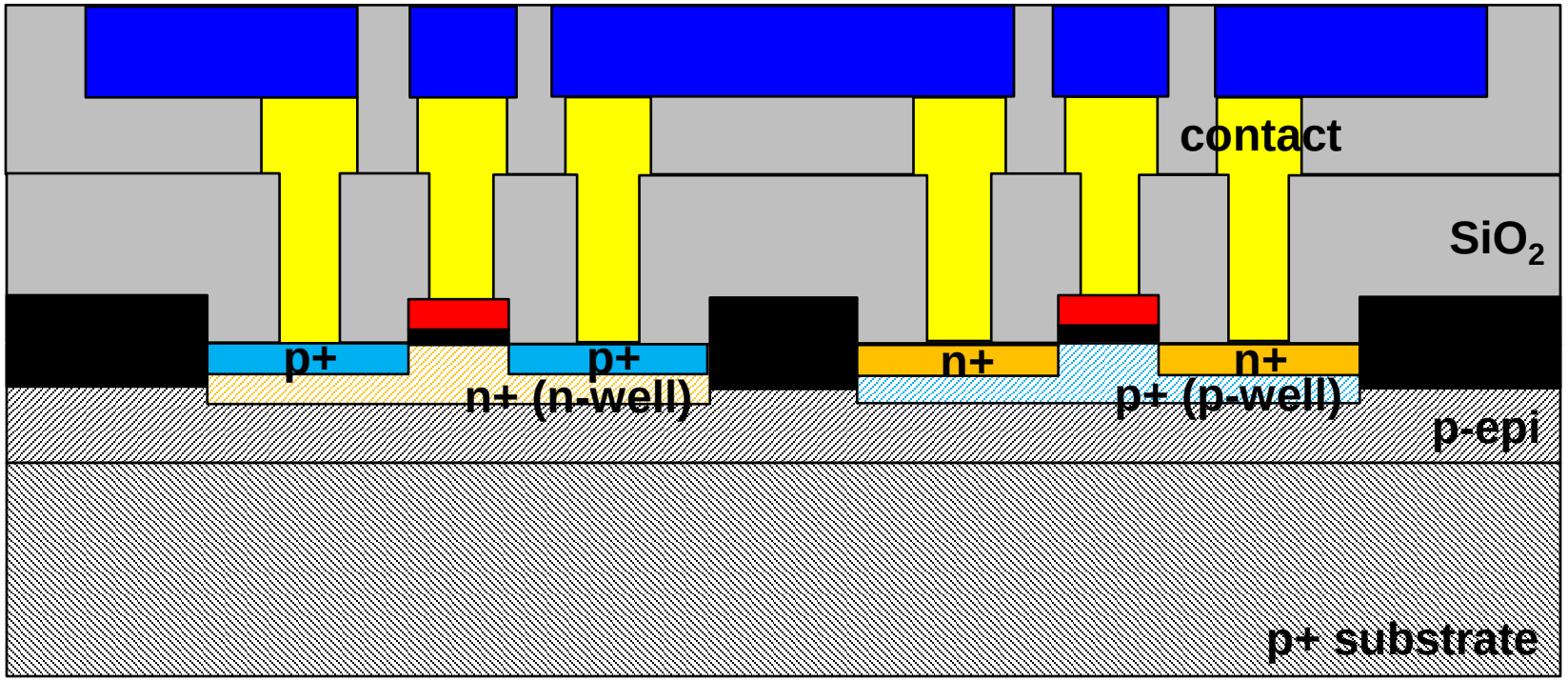
Oxide deposition

Semiconductor Manufacturing



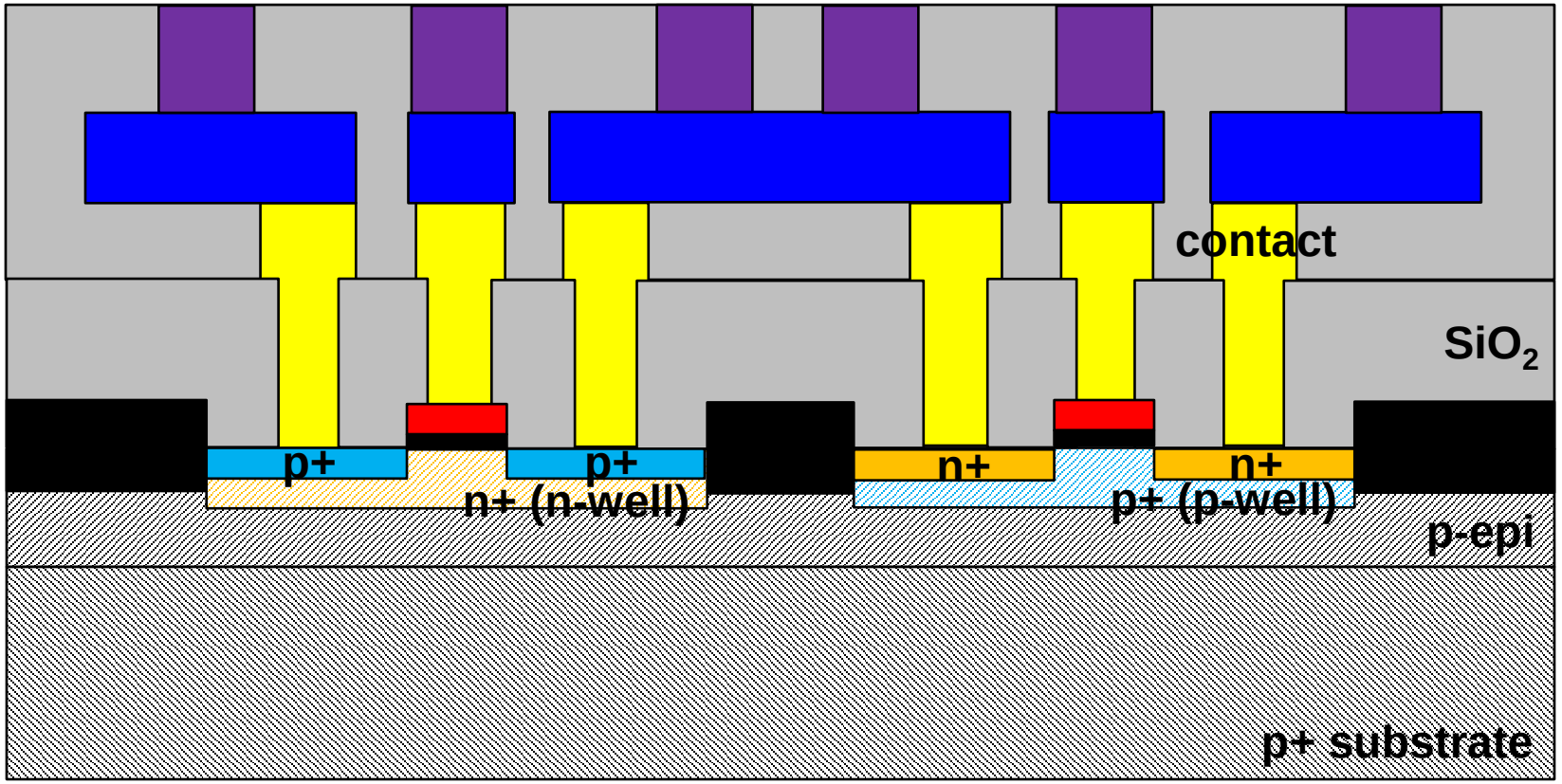
Contact

Semiconductor Manufacturing



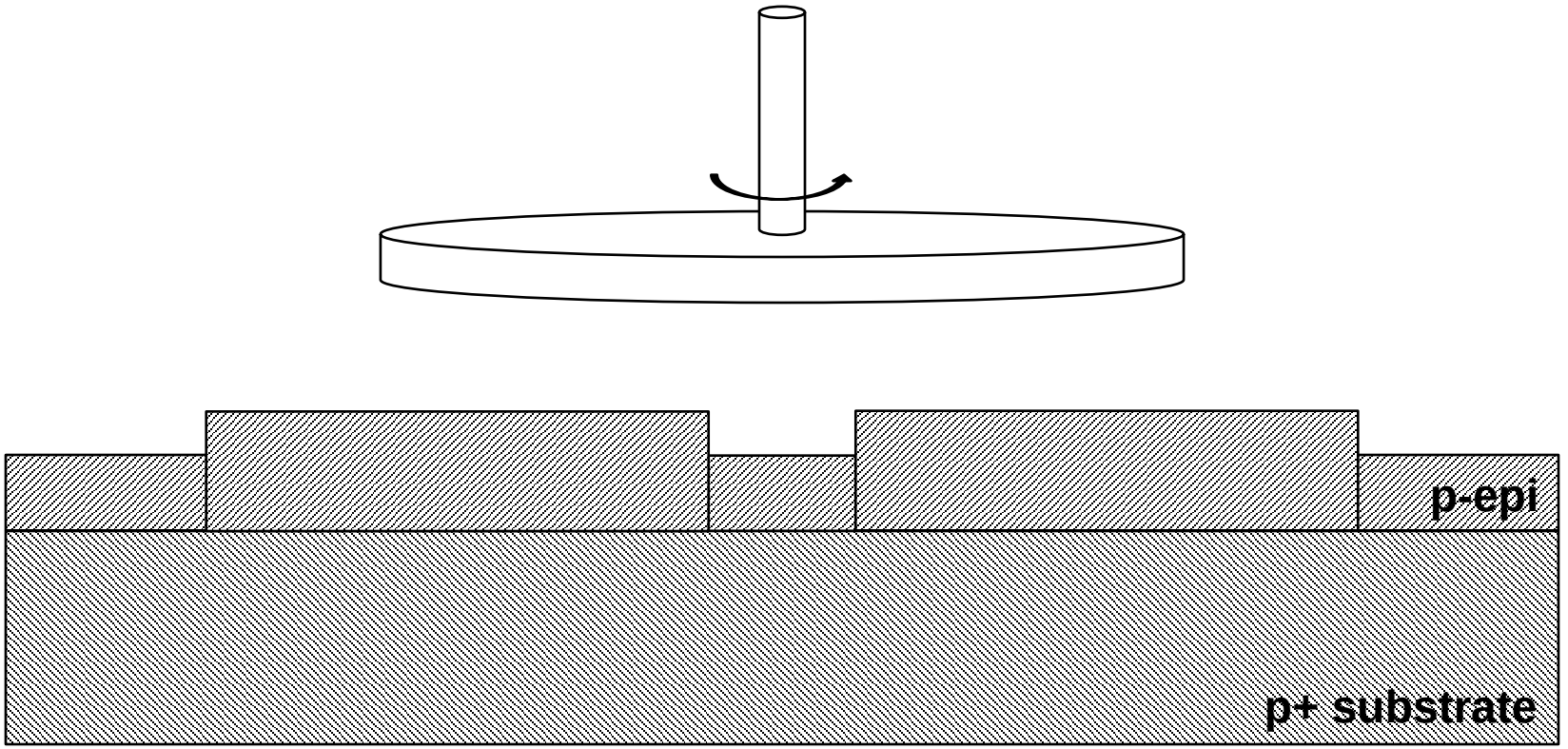
Metal 1

Semiconductor Manufacturing



Via12

Semiconductor Manufacturing



Chemical-mechanical-polishing (CMP)

Semiconductor Manufacturing