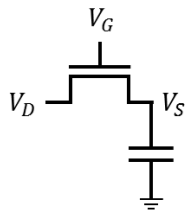
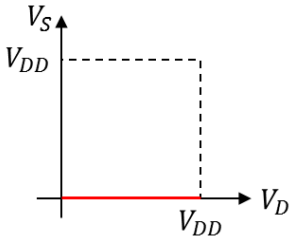
Homework Assignment 1
(Due 4:10pm, Jan. 25)

[Transistor Characteristics] Assume that $V_{tn} \approx V_{DD}/4$.

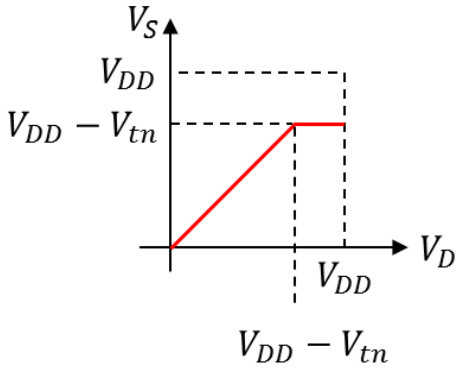


(1) [10 points] Draw a graph of V_D (x-axis) vs. V_S (y-axis) for $V_G = 0$.



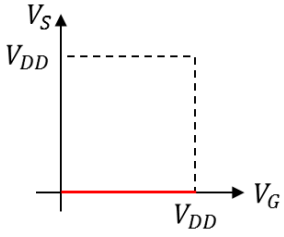
If V_G is 0V, the NFET is always turned off, so V_S holds the initial value.

(2) [10 points] Draw a graph of V_D (x-axis) vs. V_S (y-axis) for $V_G = V_{DD}$.



If $V_G = V_{DD}$, the NFET is turned on only when $V_S \leq V_{DD} - V_{tn}$ is satisfied. When the NFET is turned on, the drain and the source terminals are connected, so $V_S = V_D$.

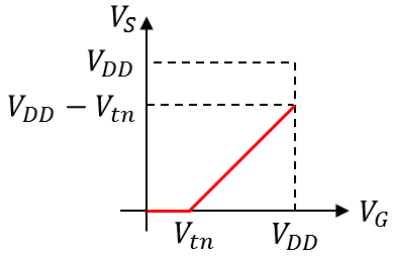
(3) [10 points] Draw a graph of V_G (x-axis) vs. V_S (y-axis) for $V_D = 0$.



Assume $V_S = 0\text{V}$. If $V_G < V_{tn}$, the NFET is turned off, so V_S is 0V. If $V_G > V_{tn}$, the NET is turned on, but $V_D = 0V$, so V_S is always 0V.

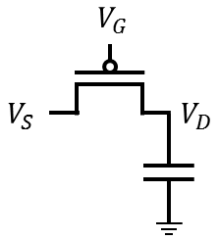
(If V_S was a certain value, it holds the value if $V_G < V_{tn}$. If V_G is greater than V_{tn}, however, the NFET is turned on and the charges stored in the capacitor will be discharged, so V_S will be 0V).

(4) [10 points] Draw a graph of V_G (x-axis) vs. V_S (y-axis) for $V_D = V_{DD}$.

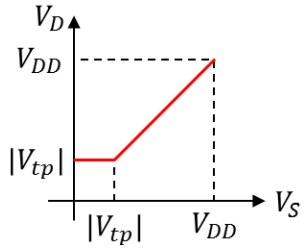


Assume $V_S = 0\text{V}$. If $V_G < V_{tn}$, the NFET is turned off, so $V_S = 0\text{V}$. If $V_G > V_{tn}$, the NFET is turned on and the capacitor will be charged. However, the NFET is turned off if $V_{GS} < V_{tn}$, i.e., $V_S > V_G - V_{tn}$.

[Transistor Characteristics] Assume that $|V_{tp}| \approx V_{DD}/4$.

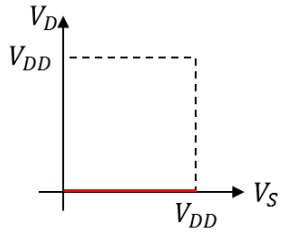


(5) [10 points] Draw a graph of V_S (x-axis) vs. V_D (y-axis) for $V_G = 0$.



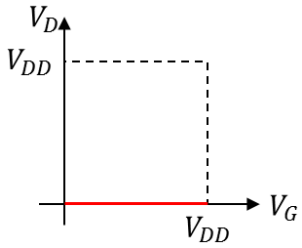
The PFET is ON if $V_{SG} > |V_{tp}|$. Since $V_G = 0\text{V}$, the PFET is ON if $V_S > |V_{tp}|$.

(6) [10 points] Draw a graph of V_S (x-axis) vs. V_D (y-axis) for $V_G = V_{DD}$.



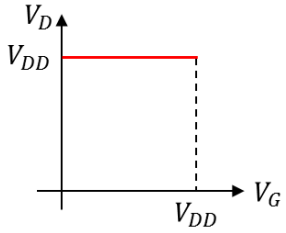
V_{SG} is always less than or equal to 0V in this case, so the PFET is always OFF. Thus, V_D holds the initial value.

(7) [10 points] Draw a graph of V_G (x-axis) vs. V_D (y-axis) for $V_S = 0$.



Assume $V_D = 0$V. Then, $V_{SG} = 0 - V_G \leq 0$V, so the PFET is always OFF. In this case, V_D holds its initial value.

(8) [10 points] Draw a graph of V_G (x-axis) vs. V_D (y-axis) for $V_S = V_{DD}$.

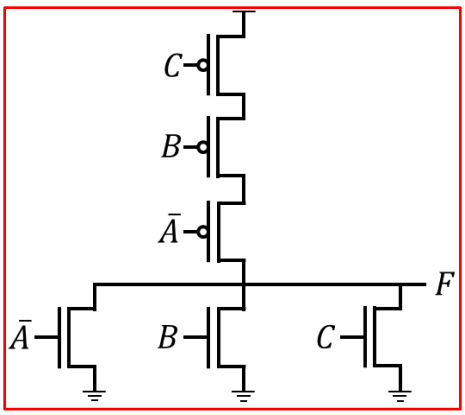


The PFET is ON if $V_{SG} = V_{DD} - V_G > |V_{tp}|$, i.e., if $V_G < V_{DD} - |V_{tp}|$. In this case, V_D will be V_{DD}. If $V_G > V_{DD} - |V_{tp}|$, the PFET is turned off and the V_D will hold the last value, which is V_{DD}.

(9) [10 points] Design the following logic using NFETs and PFETs. Available inputs: A, B, C. Try to minimize # TRs.

$$F = A \cdot (\overline{B + C})$$

$$F = A \cdot (\overline{B + C}) = \bar{\bar{F}} = \overline{\bar{A} + B + C}$$


C
B
$\bar{A}$
F
$\bar{A}$
B
C