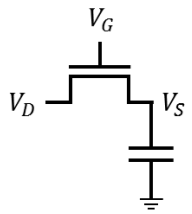
Homework Assignment 1
(Due 4:10pm, Jan. 25)

[Transistor Characteristics] Assume that $V_{tn} \approx V_{DD}/4$.



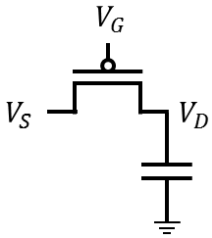
(1) [10 points] Draw a graph of V_D (x-axis) vs. V_S (y-axis) for $V_G = 0$.

(2) [10 points] Draw a graph of V_D (x-axis) vs. V_S (y-axis) for $V_G = V_{DD}$.

(3) [10 points] Draw a graph of V_G (x-axis) vs. V_S (y-axis) for $V_D = 0$.

(4) [10 points] Draw a graph of V_G (x-axis) vs. V_S (y-axis) for $V_D = V_{DD}$.

[Transistor Characteristics] Assume that $|V_{tp}| \approx V_{DD}/4$.



(5) [10 points] Draw a graph of V_S (x-axis) vs. V_D (y-axis) for $V_G = 0$.

(6) [10 points] Draw a graph of V_S (x-axis) vs. V_D (y-axis) for $V_G = V_{DD}$.

(7) [10 points] Draw a graph of V_G (x-axis) vs. V_D (y-axis) for $V_S = 0$.

(8) [10 points] Draw a graph of V_G (x-axis) vs. V_D (y-axis) for $V_S = V_{DD}$.

(9) [10 points] Design the following logic using NFETs and PFETs. Available inputs: A, B, C. Try to minimize # TRs.

$$F = A \cdot (\overline{B + C})$$