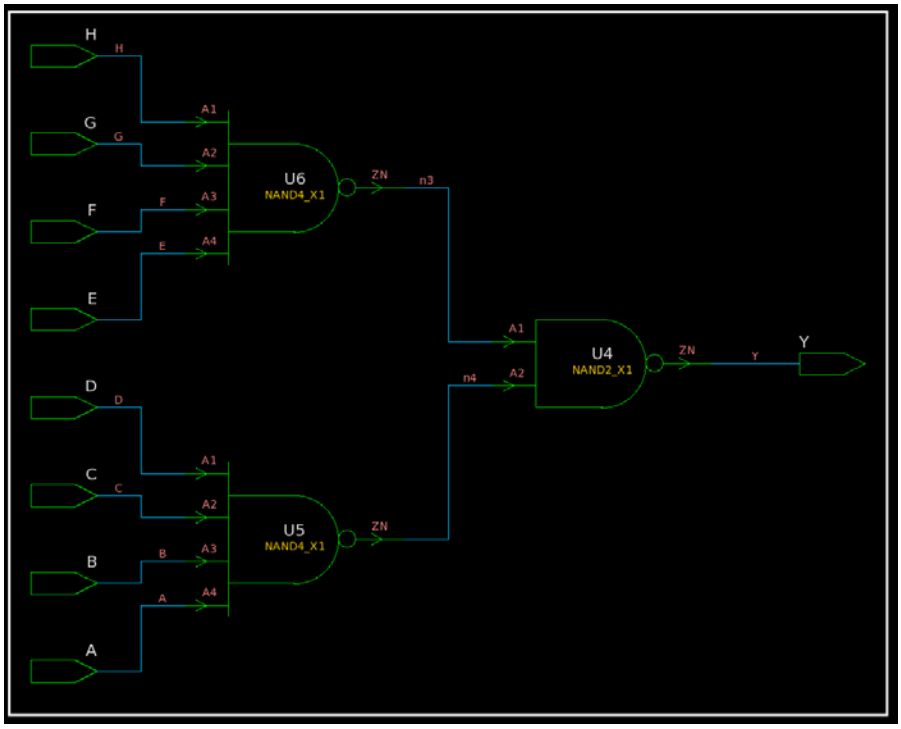
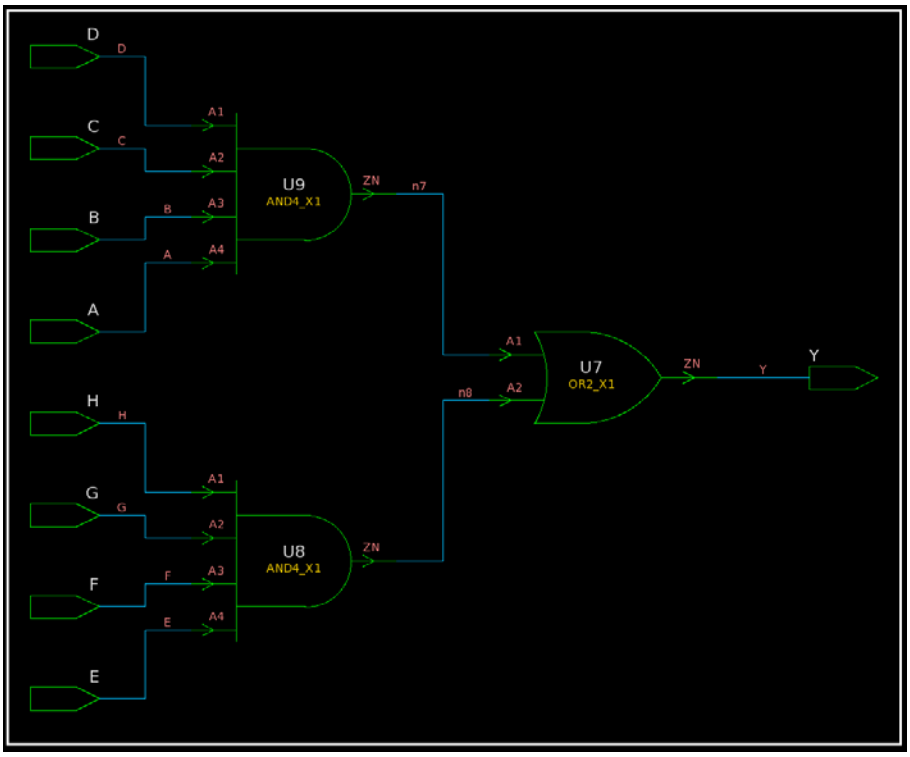
Homework Assignment 3
(Due 4:10pm, Feb. 8)

(1) [10 points] Create a Verilog code for $Y = A \cdot B \cdot C \cdot D + E \cdot F \cdot G \cdot H$. Then, synthesize it using Design Compiler. Submit 1) a screenshot of the synthesized netlist and 2) the total area.



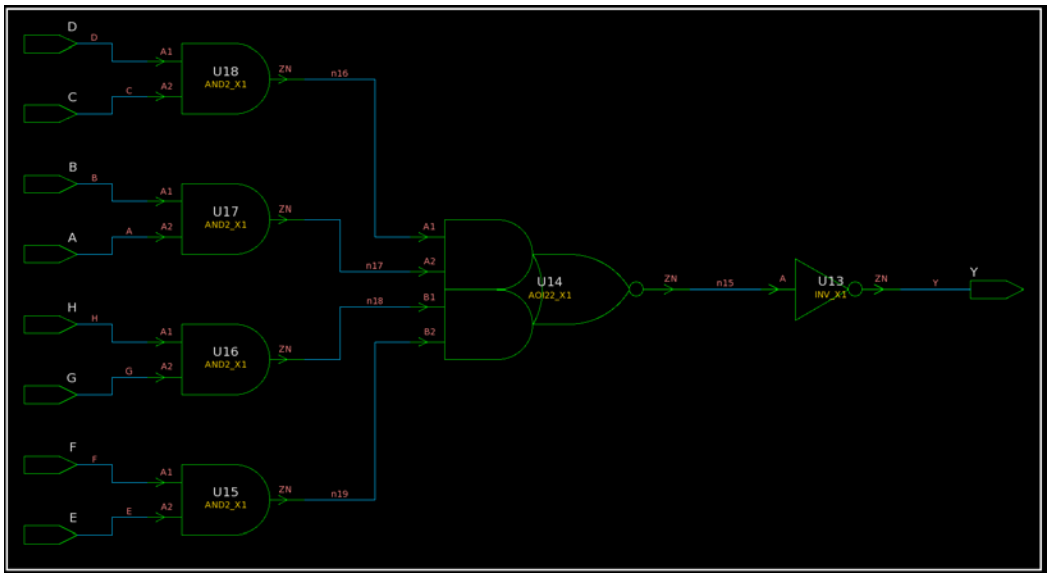
Area: 3.458um^2

(2) [10 points] Disable all the NAND gates. Use "set_dont_use {NangateOpenCellLibrary/NAND*}". Then, synthesize the netlist again. Submit 1) a screenshot of the synthesized netlist and 2) the total area.



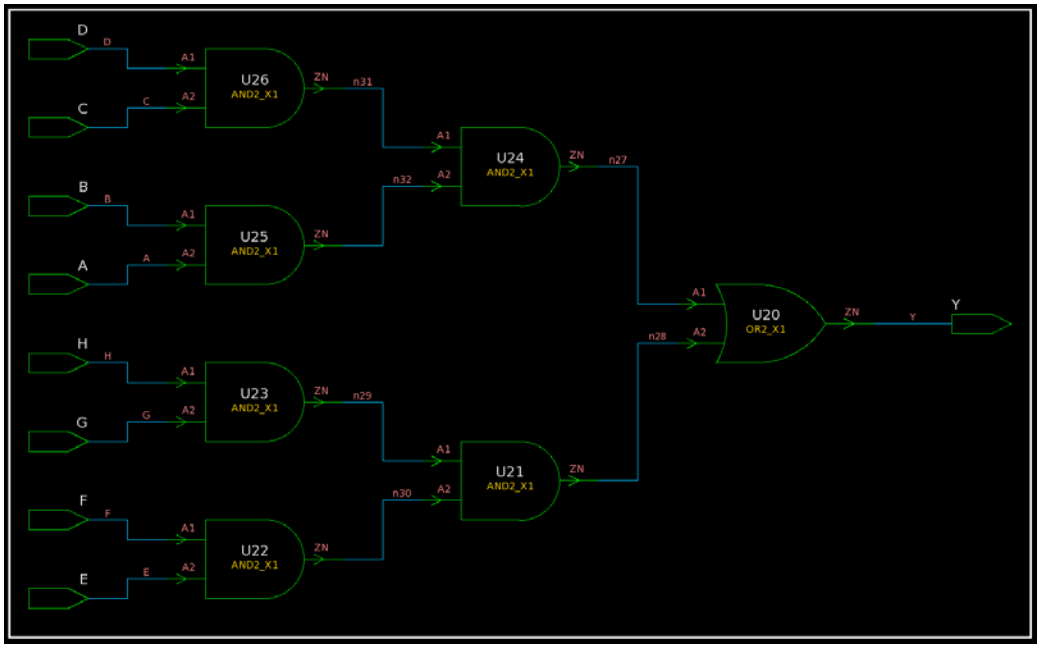
Area: 4.256 um^2

(3) [10 points] Disable all the four- and three-input gates too. Use "set_dont_use {NangateOpenCellLibrary/*3* NangateOpenCellLibrary/*4*}". Then, synthesize the netlist again. Submit 1) a screenshot of the synthesized netlist and 2) the total area.



Area: 6.118 um^2

(4) **[10 points]** Disable all the gates. Use "set_dont_use {NangateOpenCellLibrary/*}". Then, enable only two-input AND gates, two-input OR gates, and inverters. Use "remove_attribute {NangateOpenCellLibrary/AND2_* NangateOpenCellLibrary/OR2_* NangateOpenCellLibrary/INV_*} DONT_USE". Then, synthesize the netlist again. Submit 1) a screenshot of the synthesized netlist and 2) the total area.



Area: 7.448 um^2