Homework Assignment 3
(Due 4:10pm, Feb. 8)

[Synthesis] Download and unzip http://eecs.wsu.edu/~ee434/Homework/hw03.zip. You will see the following files:

- nangate.db: Nangate 45nm standard cell library
- test.v: Test Verilog code
- test.tcl: Test synthesis script

Follow the instructions in hw00.pdf to source "ictools_generic.sh" and "synopsys.sh".

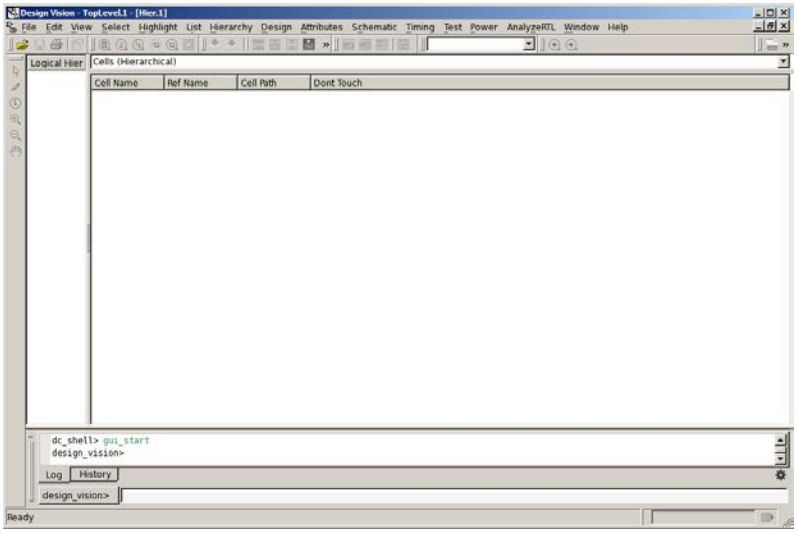
Open test.v in a text editor and see the Verilog code. It implements $Y = A \cdot B + C \cdot D$.

Open test.tcl in a text editor and see the scripts. It sets up target libraries (Line 1, 2), reads a given Verilog code (Line 4), sets the current design to the top-level design (Line 6, since there is only one module in test.v, we don't need this line, but I just included it), synthesizes the Verilog code (Line 8), and saves the synthesis result into test_syn.v (Line 10).

Run Design Compiler as follows:

- design_vision

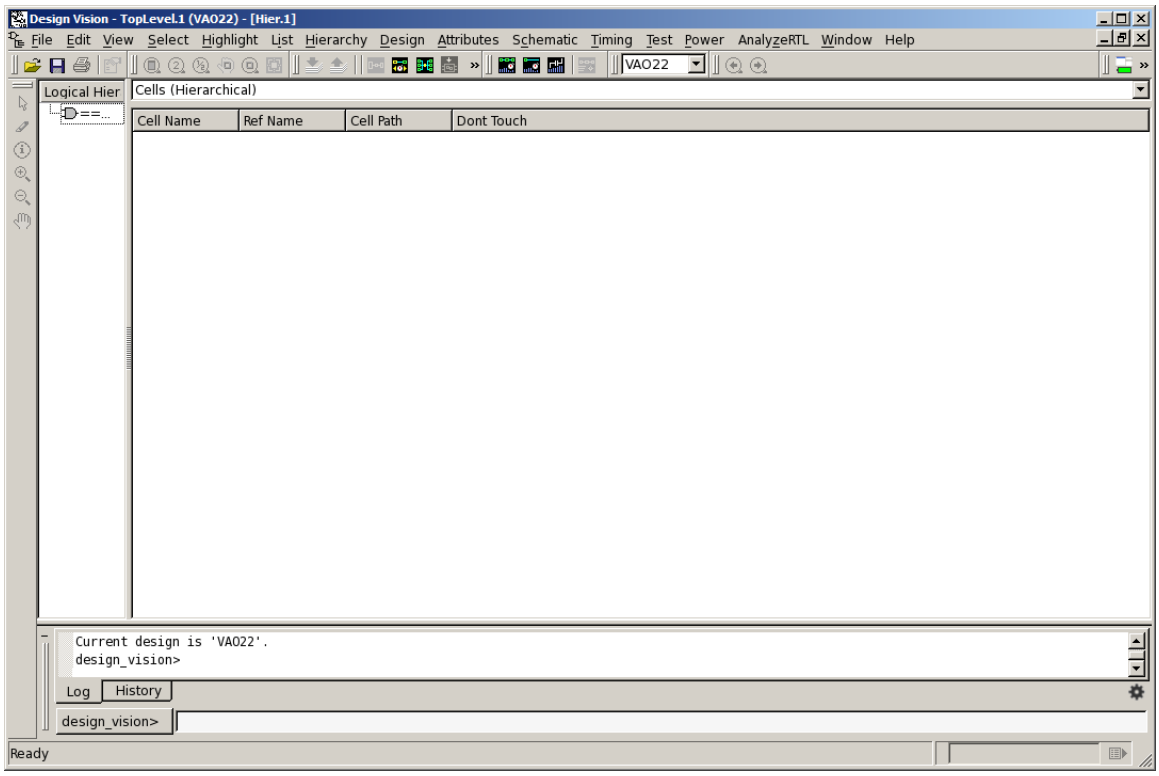
This will show you a design_vision GUI as follows:



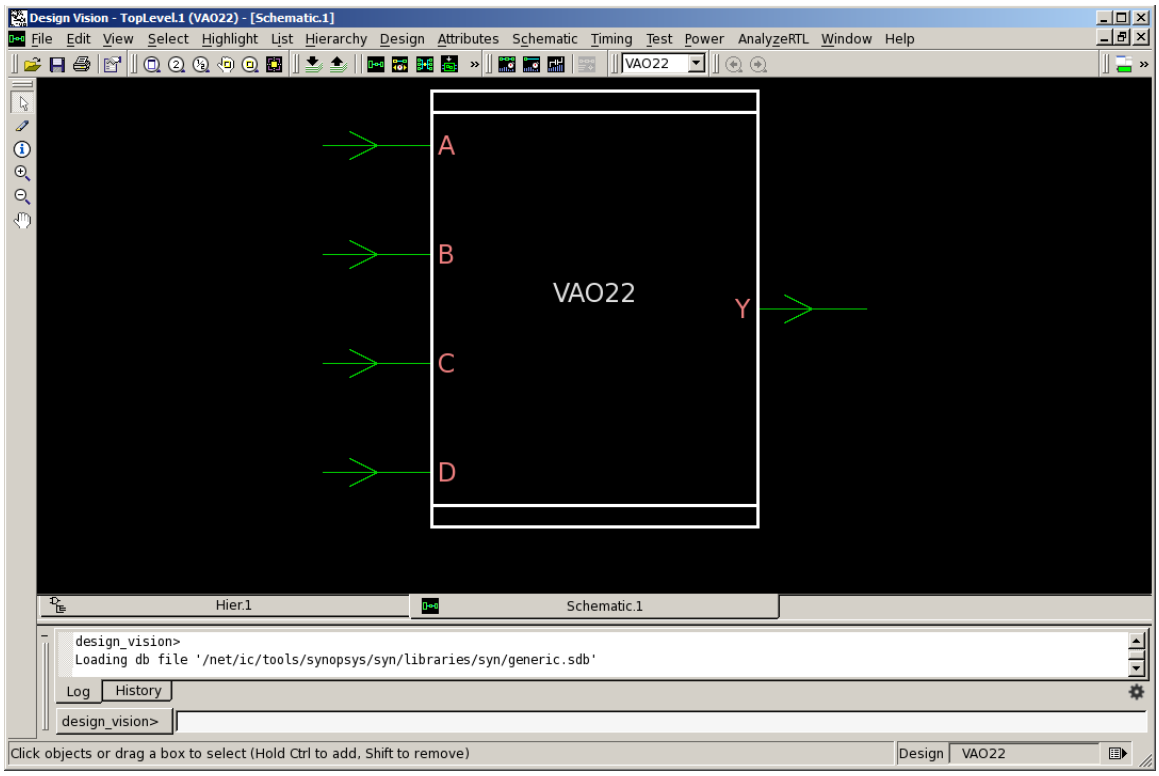
Go back to your terminal. You can enter commands in the terminal. Run the following command:

- source test.tcl

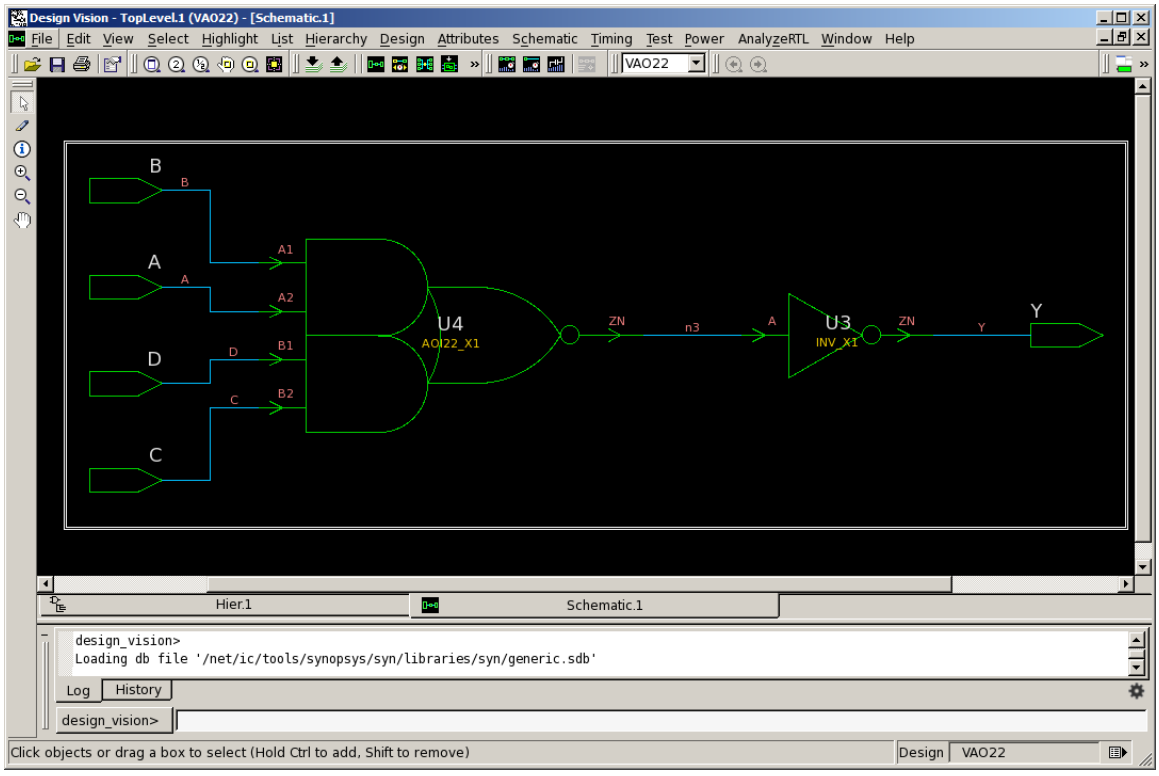
This will run all the commands in test.tcl. Once it is done, you will see the following window:



Click the gate symbol under “Logical Hierarchy”. Then, click Schematic → New Schematic View.



Double-click the module. You will see the following:



Open test_syn.v in a text editor. This shows the synthesized netlist. You will see that it uses an AOI22_X1 cell (implementing $\overline{A1 \cdot A2 + B1 \cdot B2}$) and an inverter cell.

Let’s get the area of the synthesized netlist. Run the following command:

- report_area

I got this:

Combinational area: 1.862

Buf/Inv area: 0.532

Total cell area: 1.862

The unit is um^2.

Now, suppose you don’t want to use the AOI22 cell in the standard cell library. Let’s disable it. Use the following command:

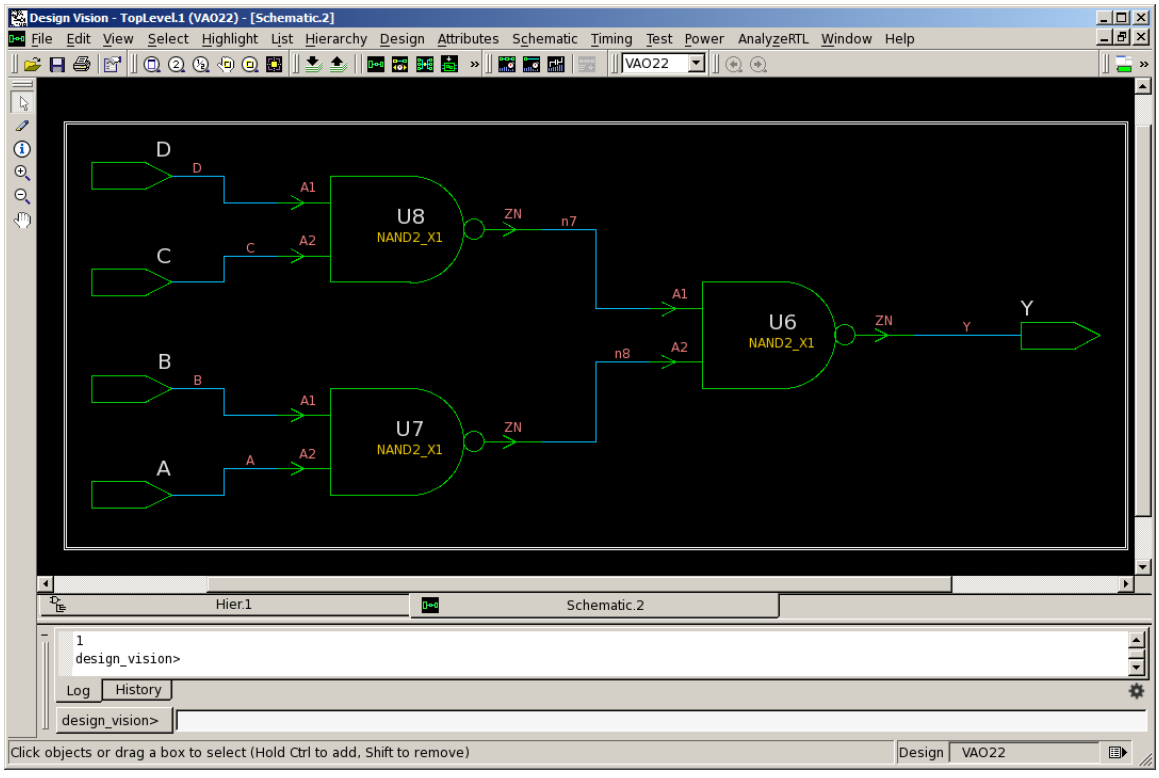
- set_dont_use {NangateOpenCellLibrary/AOI22*}

This disables using all the cells whose names begin with “AOI22”.

Then, let’s re-synthesize the current netlist. Run the following command:

- compile -exact_map -map_effort high

Open a new schematic view. It will show you the following:



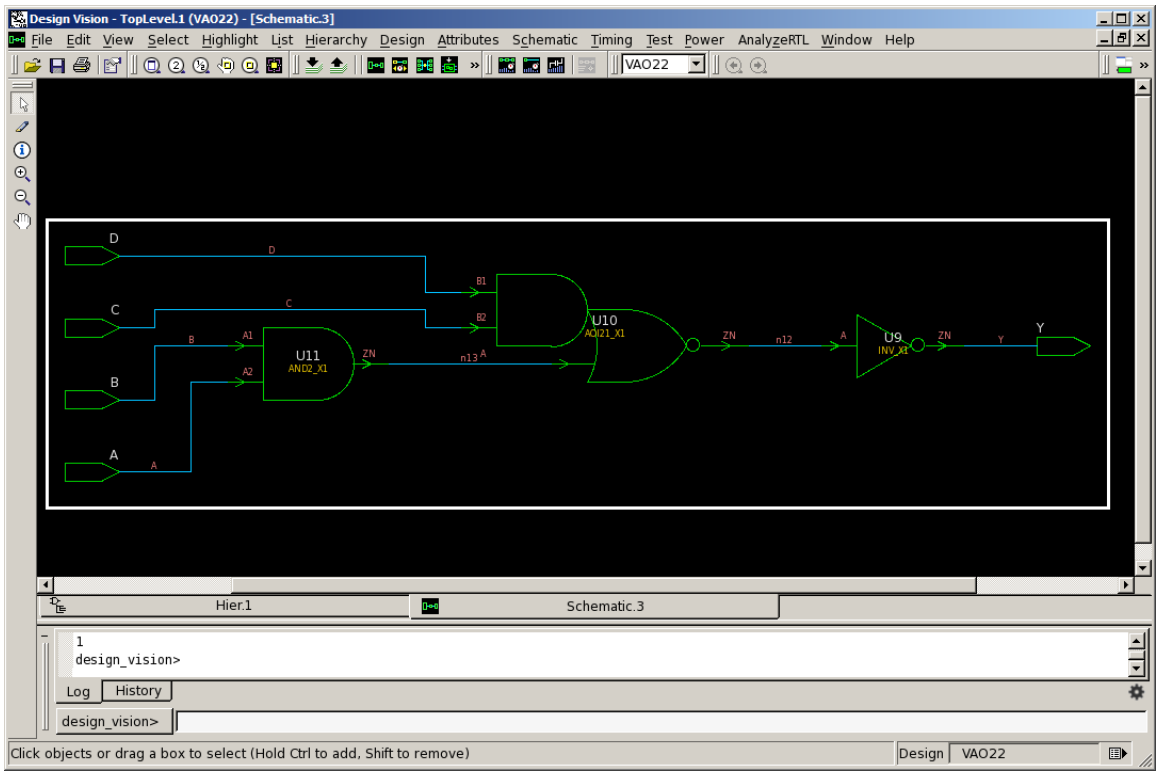
Now, it uses three two-input NAND gates. Let’s get the total area.

- report_area

The total area I got is 2.394, which is greater than 1.862.

Let’s disable two-input NAND gates too.

- set_dont_use {NangateOpenCellLibrary/NAND2*}
- compile –exact_map –map_effort high



Total area: 2.66

(1) [10 points] Create a Verilog code for $Y = A \cdot B \cdot C \cdot D + E \cdot F \cdot G \cdot H$. Then, synthesize it using Design Compiler. Submit 1) a screenshot of the synthesized netlist and 2) the total area.

(2) [10 points] Disable all the NAND gates. Use “set_dont_use {NangateOpenCellLibrary/NAND*}”. Then, synthesize the netlist again. Submit 1) a screenshot of the synthesized netlist and 2) the total area.

(3) [10 points] Disable all the four- and three-input gates too. Use “set_dont_use {NangateOpenCellLibrary/*3* NangateOpenCellLibrary/*4*}”. Then, synthesize the netlist again. Submit 1) a screenshot of the synthesized netlist and 2) the total area.

(4) **[10 points]** Disable all the gates. Use “set_dont_use {NangateOpenCellLibrary/*}”. Then, enable only two-input AND gates, two-

input OR gates, and inverters. Use “remove_attribute {NangateOpenCellLibrary/AND2_* NangateOpenCellLibrary/OR2_* NangateOpenCellLibrary/INV_*} DONT_USE”. Then, synthesize the netlist again. Submit 1) a screenshot of the synthesized netlist and 2) the total area.