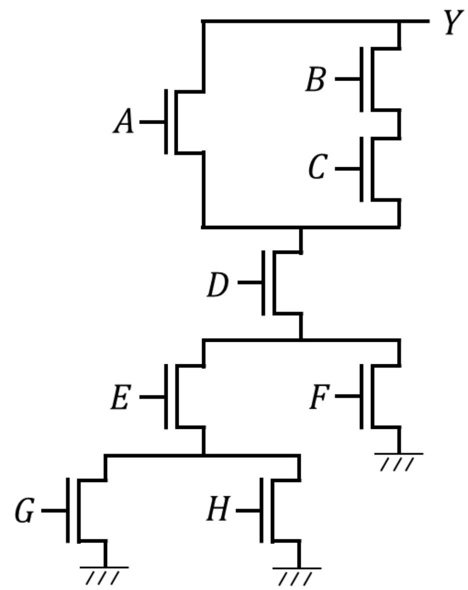
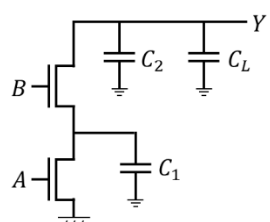
Homework Assignment 5
(Due 4:10pm, Feb. 25)

(1) [Transistor Sizing, 20 points] The following shows a schematic of the NFET network of a static CMOS gate. Size the transistors so that the fall delay is less than or equal to $R_n C_L$ where R_n is the resistance of a 1X NFET and C_L is the load capacitance. Try to minimize the total width. Find the total width.



(2) [Transistor Sizing, 40 points] The following shows a schematic of the NFET network of a static CMOS two-input NAND gate. C_L is a load capacitance. If we upsize the transistors, the drain and source capacitances increase. For more accurate transistor sizing, therefore, the figure shows two more capacitors, C_1 and C_2. Find optimal sizes of transistor A and B minimizing the total area for timing constraint $\tau_T = (d+2)R_n c_0$. See below for more details.



- Size of TR A: s_1 (variable. You should find the optimal value of this variable.)
- Size of TR B: s_2 (variable. You should find the optimal value of this variable.)

- R_n: The resistance of a $1 \times$ NFET (constant)
- c_0: A unit capacitance (constant)
- $C_1 = c_0 \cdot (s_1 + s_2)$
- $C_2 = c_0 \cdot s_2$
- $C_L = c_0 \cdot k$ (constant, k is also a constant)
- Timing constraint: Delay = $\tau_T = (d + 2)R_n c_0$ (constant, d is also a constant)
- The delay of the pull-down logic: $\tau = R_2 \cdot (C_2 + C_L) + R_1 \cdot (C_1 + C_2 + C_L)$
- Total area: $s_1 + s_2$

You can follow the instructions below:

1) You should satisfy the target timing constraint, which gives you an equation. Get the equation from the constraint, i.e., get an equation $f(s_1, s_2, R_n, c_0, k, d) = 0$ from $\tau = \tau_T$. The equation will look like this: $s_1 = \frac{\square \cdot {s_2}^2 + \square \cdot s_2}{\square \cdot s_2 - \square}$
2) The total area is $A = s_1 + s_2$. Substitute s_1 into A so that A is expressed as a single-variable function. Differentiate A w.r.t. s_2 and set it to zero. It will give you two roots, $s_2 = 0$ and $s_2 = X$. Find X. It will look like this: $s_2 = \frac{\square \cdot k}{d}$.
3) Find s_1. It will look like $s_1 = \frac{\square \cdot k \cdot (d + \square)}{d^2}$.