Homework Assignment 1
(Due 4pm, Jan. 17th, email to daehyun@eecs.wsu.edu)

(1) **[Design Compiler, 20 points]** If you have not set up your Linux account, go to the IT help desk (on the 3rd floor of Sloan) and create an account. Then, log in to your Linux account (see the ***tutorial_linux.pdf*** in the "Lab" directory in the class website) and create a directory for this homework. Download the following file to the directory.

- http://eecs.wsu.edu/~ee434/Homework/hw01.zip

You can use the following command to download it into the directory.

- wget eecs.wsu.edu/~ee434/Homework/hw01.zip

Unzip it.

- Unzip hw01.zip

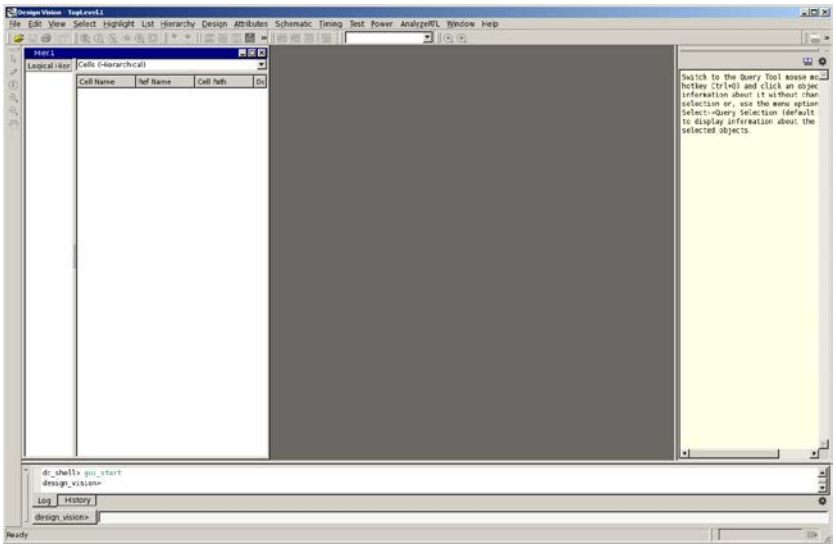
Source the two sh files as follows:

- source ictools_generic.sh
- source synopsys.sh

Then, run design compiler (DC) as follows:

- design_vision –output_log_file "your_id#.log"
- (for example, design_vision –output_log_file 012345678.log)

You will see the main GUI window of DC.



If you don’t see this window, you didn’t properly set up the GUI environment. See tutorial_linux.pdf or just go to EME205 and use a Linux desktop in the lab.

Now, go back to your terminal. You will see a prompt as follows:

```
design_vision> design_vision>
design_vision>
design_vision>
```

Type “source a.tcl” and enter. It will load a.tcl and execute the commands in the file.

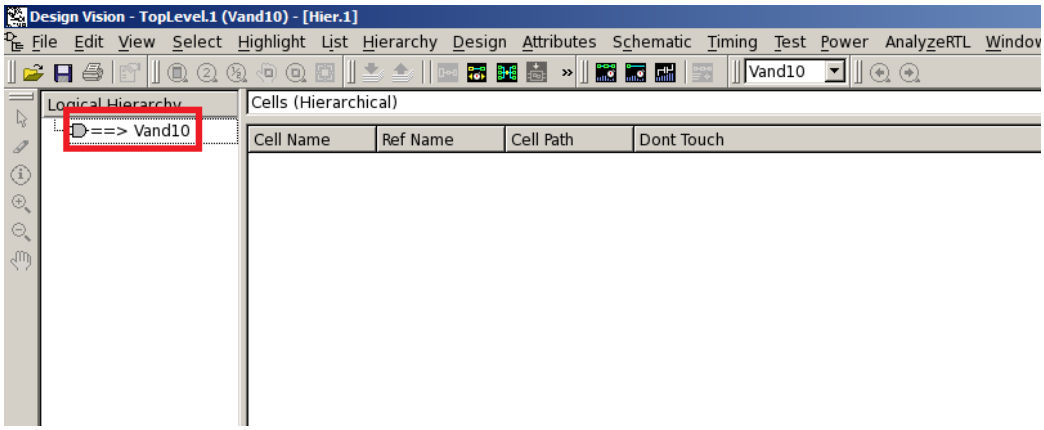
```
   ELAPSED            WORST NEG   SETUP    DESIGN
    TIME      AREA      SLACK     COST    RULE COST         ENDPOINT
  --------- --------- --------- --------- --------- -------------------------
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
    0:00:01       5.1      0.00       0.0       0.0
Loading db file '/net/fs/daehyun/pvt/course/2018_Spring/hw01/ng45.db'


Note: Symbol # after min delay cost means estimated hold TNS across all active scenarios


  Optimization Complete
  ---------------------
Writing verilog file '/net/fs/daehyun/pvt/course/2018_Spring/hw01/and10_syn.v'.
1
Current design is 'Vand10'.
design_vision>
```

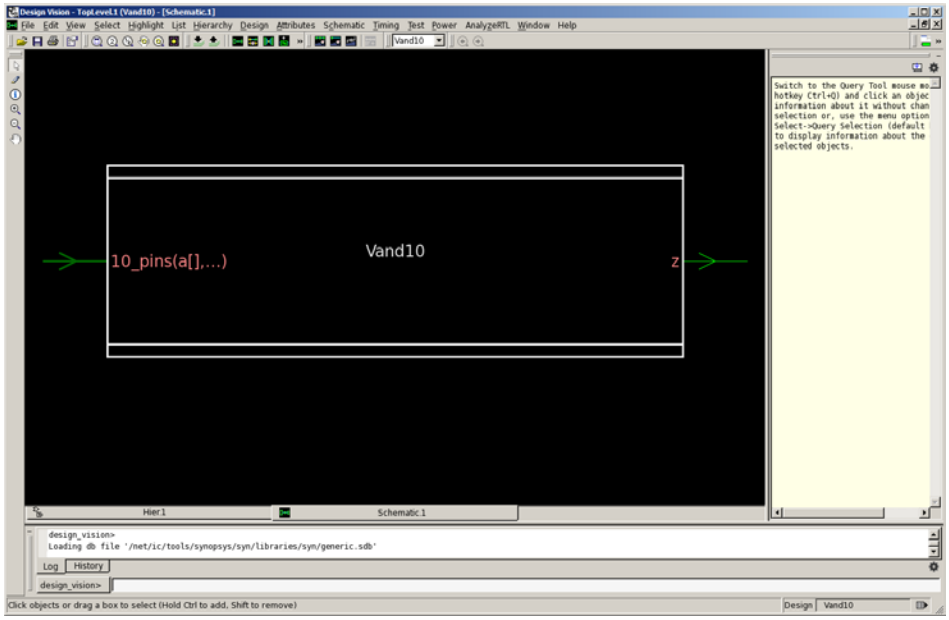
You’ve just synthesized a 10-input AND gate.

Go to the GUI window and click “Vand10”, which is the name of the 10-input AND gate.



If you click it, it will be highlighted with a blue rectangle.

In the main menu, click “Schematic” and “New Schematic View”. You will see something like this:



Double-click the Vand10 rectangle and you will see a schematic (netlist, connections of gates). Screen-capture the schematic.

Exit DC by typing “exit”. You will see the log file “your_id#.log” in your directory.

[**Submit**] Zip the log file and the schematic image file into “hw01_your_id#.zip” (e.g., hw01_012345678.zip) and submit it by email.