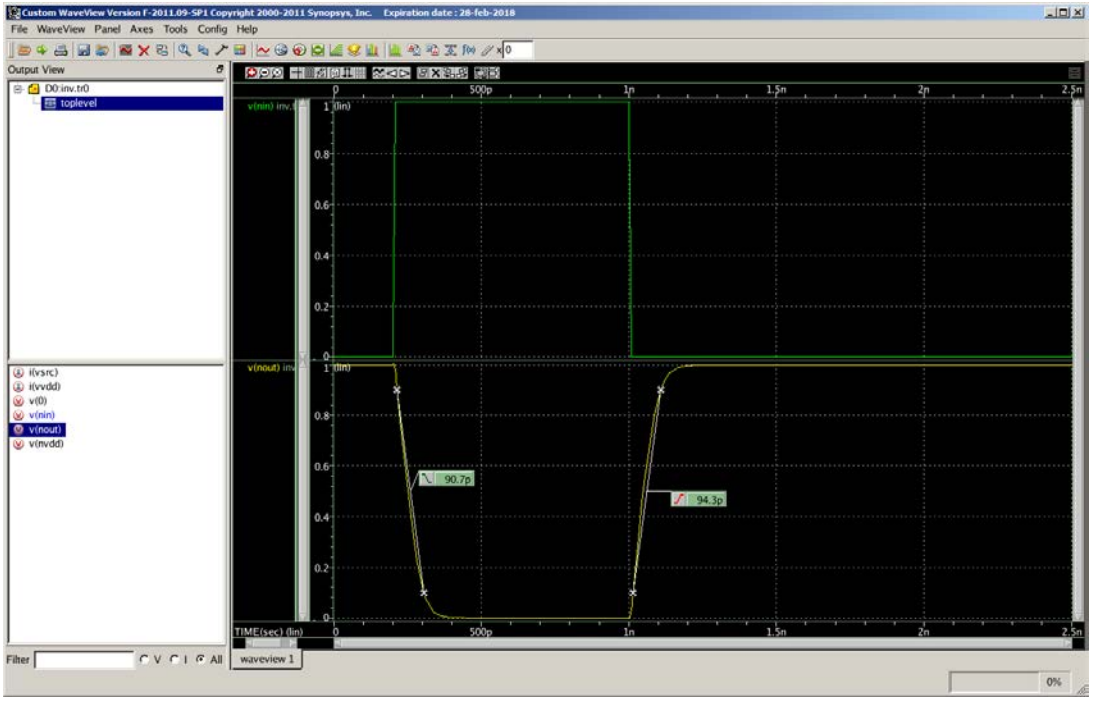
Homework Assignment 2
(Due 5pm, Jan. 24, email to daehyun@eecs.wsu.edu)

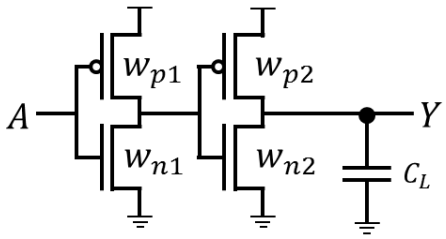
(1) **[Inverter, 10 points]** Open ***tutorial-hspice.pdf*** in the "Lab" webpage and try to run HSpice yourself. Change the width of the NFET from 50n to 100n and that of the PFET from 75n to 150n and rerun HSpice. Measure the rise time and the fall time.

- [**Submit**] Screen-capture the input and output waveforms with the rise and fall times shown on the waveform.



Rise time: 94.3ps, Fall time: 90.7ps

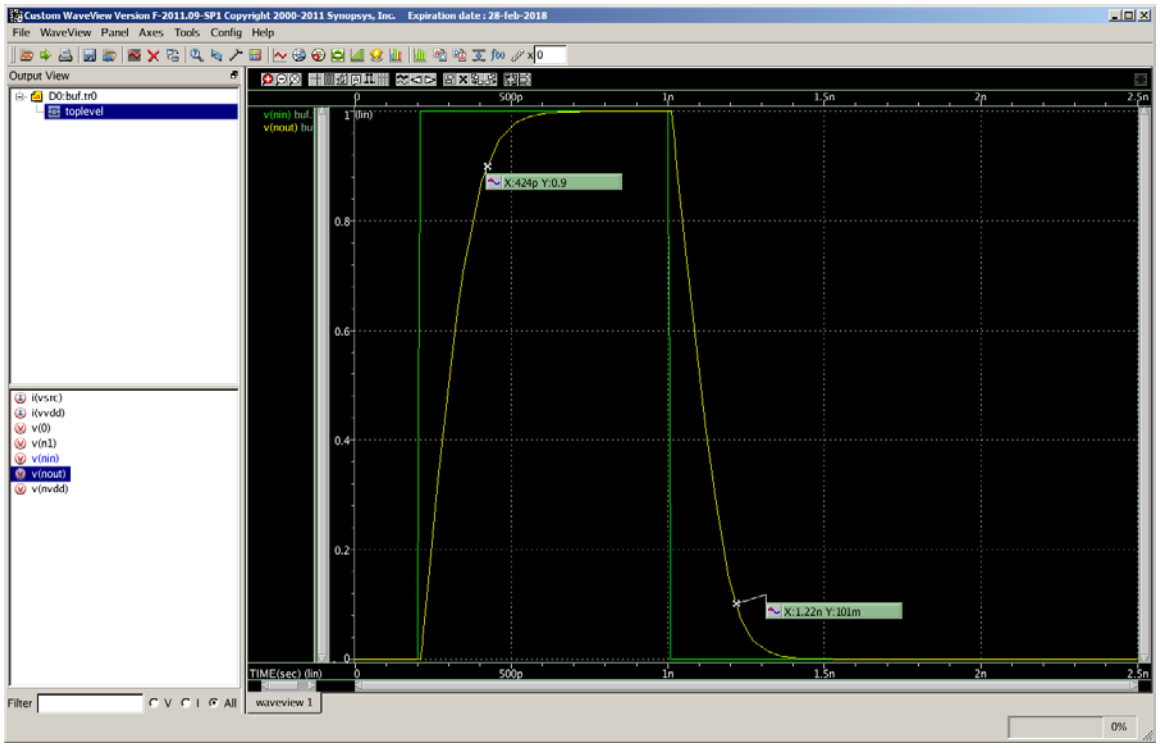
(2) [**Buffer, 10 points**] Create a netlist to simulate a buffer. A buffer consists of two inverters as follows (w is the width of the transistor):



Notice that all the transistors should have the minimum length (45nm).

- Specification: $w_{n1} = w_{n2} = 50n$, $w_{p1} = w_{p2} = 75n$, $C_L = 10fF$.

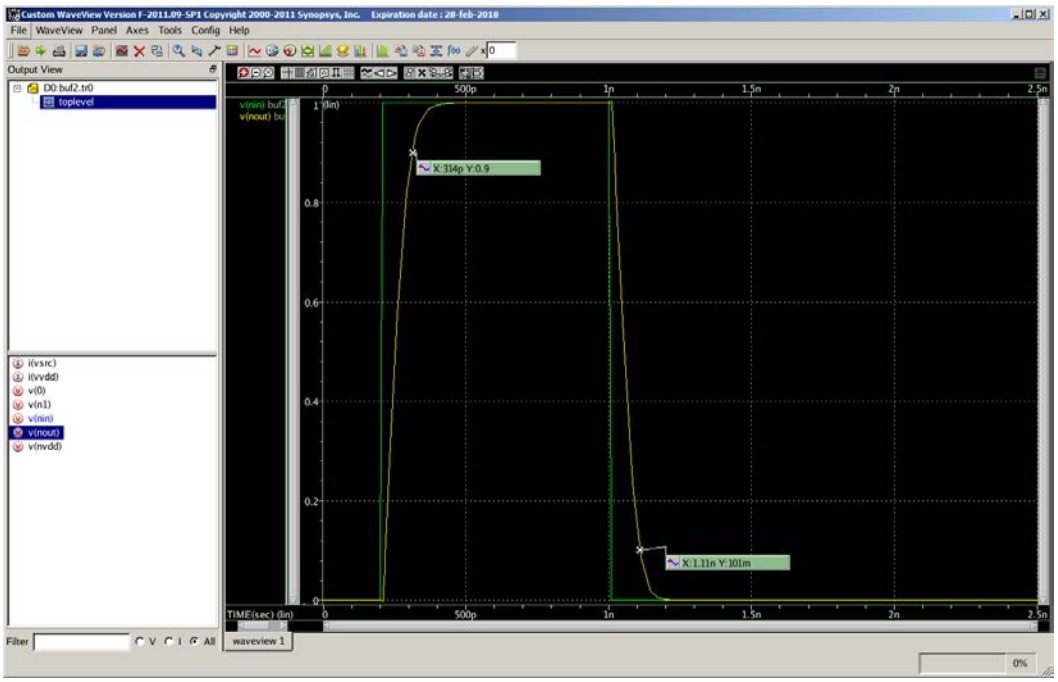
- Measure the rise and fall delays at the output.
- The rise delay is defined by $b - a$ where b is the time when the output signal Y is 0.9V and a is the time when the input signal A starts switching.
- The fall delay is defined by $b - a$ where b is the time when the output signal Y is 0.1V and a is the time when the input signal A starts switching.
- Use the "Data(X,Y)" measurement tool in the waveview.
- You can merge two waveforms by drag and drop.
- [**Submit**] Screen-capture the input and output waveforms with the rise and fall delays shown on the waveform (show the two points where the output signal is 0.9V and 0.1V).



Rise delay: 224ps, Fall delay: 220ps

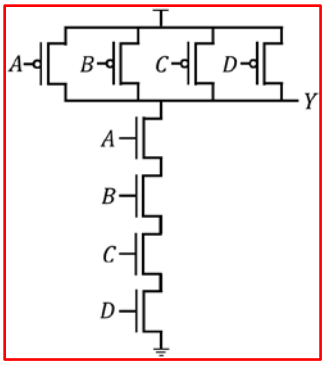
(3) [**Buffer, 10 points**] Repeat problem 2 with the following transistor width values.

- Specification: $w_{n1} = w_{n2} = 100n$, $w_{p1} = w_{p2} = 150n$, $C_L = 10fF$.
- [**Submit**] Screen-capture the input and output waveforms with the rise and fall delays shown on the waveform (show the two points where the output signal is 0.9V and 0.1V).



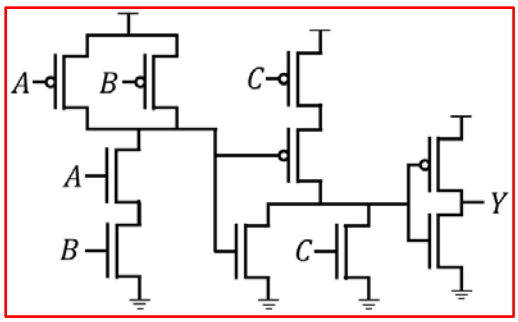
Rise delay: 114ps, Fall delay: 110ps

(4) [**Design, 5 points**] Draw a transistor-level schematic of a four-input NAND gate using four NFETs and four PFETs. Input: A, B, C, D. Output: Y.



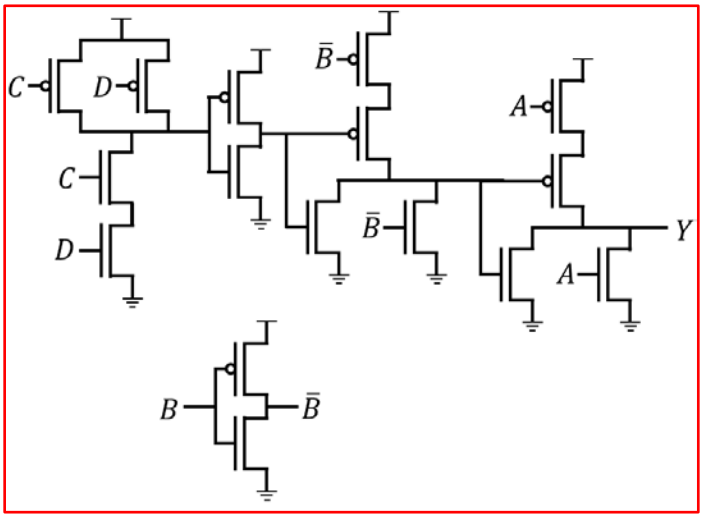
(5) [**Design, 10 points**] Draw a transistor-level schematic of $Y = \overline{A \cdot B} + C$. Available inputs: A, B, C.

$$Y = \overline{\overline{A \cdot B} + C}$$



(6) [**Design, 15 points**] Draw a transistor-level schematic of $Y = \bar{A} \cdot (\bar{B} + C \cdot D)$. Available inputs: A, B, C, D.

$$Y = \overline{A + \overline{(\bar{B} + C \cdot D)}}$$



Zip the screen shots into "hw02_your_id#.zip" (e.g., hw02_012345678.zip) and submit it by email. You can also submit problem 4–6 electronically (by taking photos and submitting it with the screen shots) or solve them on paper and submit it.