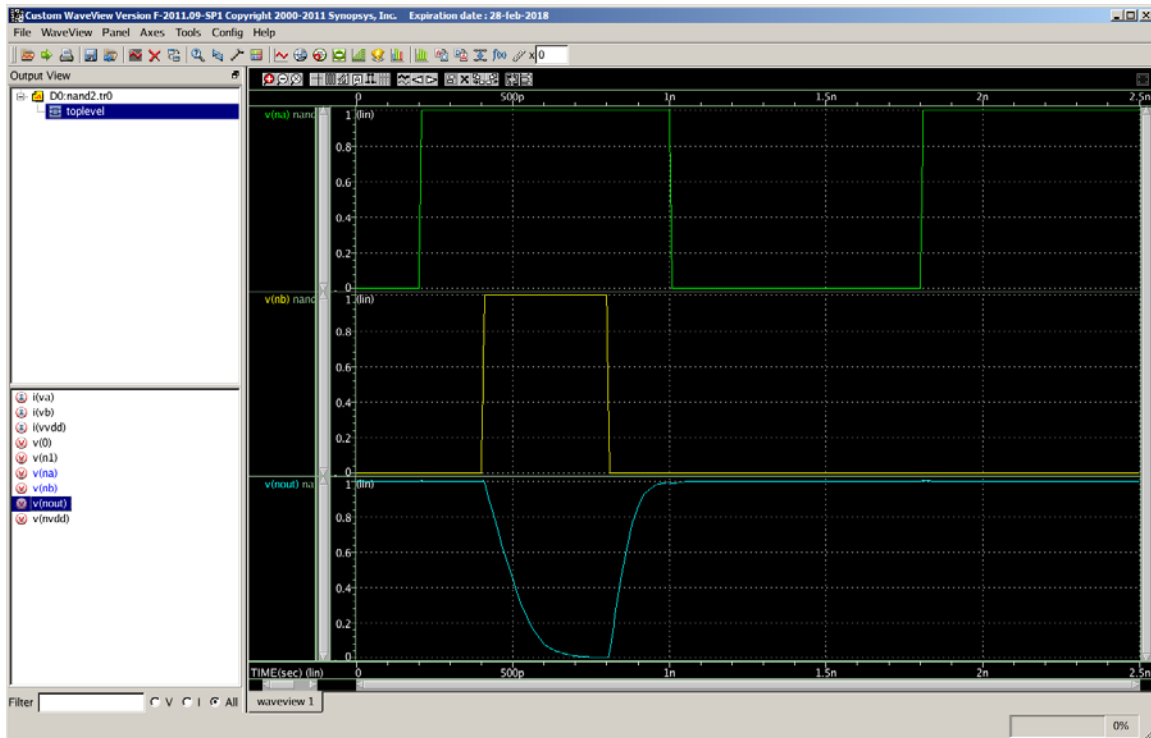# Homework Assignment 3
## (Due 5pm, Jan. 26, email to daehyun@eecs.wsu.edu)

(1) **[SPICE, 10 points]** Download hw03.zip and unzip it. You will see nand2.sp. Open it in a text editor and see the netlist. It implements a two-input NAND gate. Simulate it using HSpice and see the waveform.

- [**Submit**] Screen-capture the waveforms of the two inputs (nA and nB) and the output (nOut).

(2) [**SPICE, 10 points**] Open subckt-nand2.sp in a text editor and see the subckt definition. It defines a subckt for a two-input NAND gate. Now, open nand2-subckt.sp and see how a two-input NAND gate is instantiated. Simulate it using HSpice and see the waveform.

- [**Submit**] Screen-capture the waveforms of the two inputs (nA and nB) and the output (nOut).
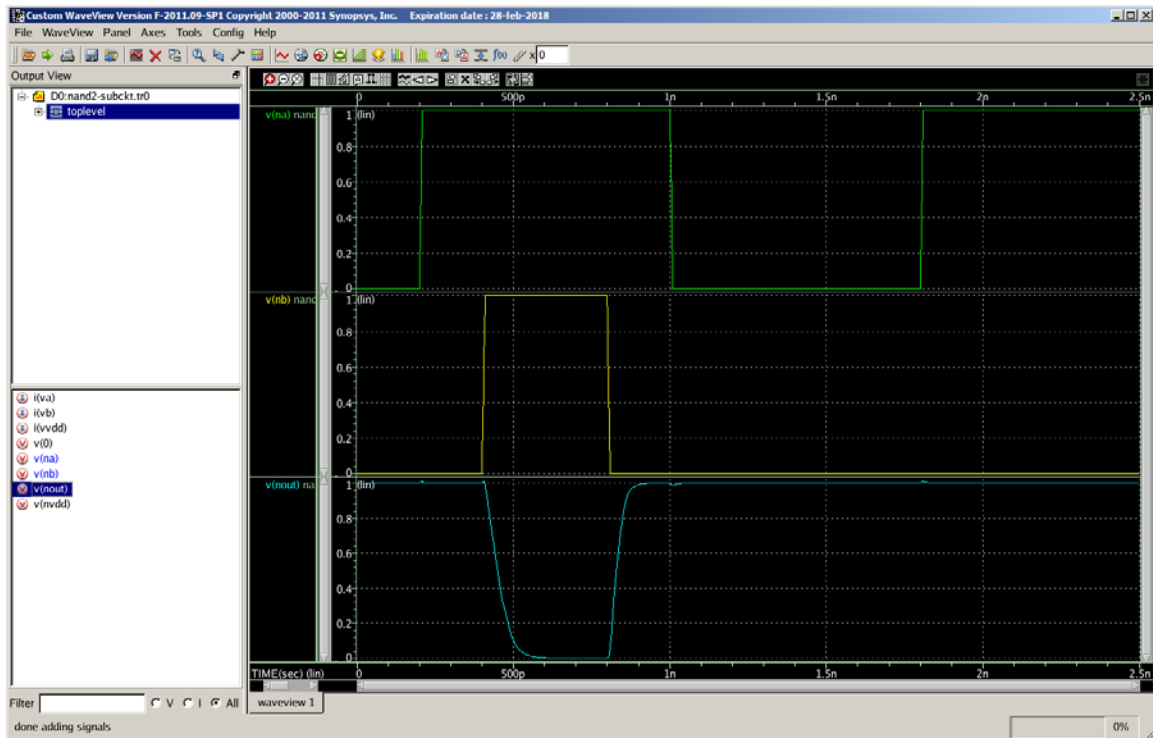
(3) [**SPICE, 20 points**] Create a subckt for a two-input NOR gate. Use L=45nm and W=50nm for the NFETs. Use L=45nm and W=300nm for the PFETs. Then, instantiate three two-input NOR gates as follows:
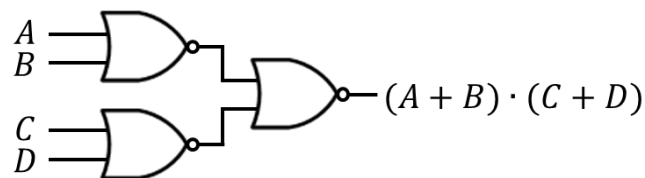
The load capacitance at the output node is 10fF. Generate input signals and simulate all the 16 input combinations (from 0000 to 1111). Make sure the output signal swings between 0 and 1 (if your implementation is not correct, the output might not reach 0V or 1V).

- [**Submit**] Screen-capture the waveforms of the four inputs (A, B, C, D) and the output. You also need to submit your HSpice netlist files.

.subckt myNor2 npA npB npOut npVdd npGnd

mn1 npOut npA npGnd npGnd NMOS_HP L=45n W=50n

mn2 npOut npB npGnd npGnd NMOS_HP L=45n W=50n

mp1 npOut npA n1 npVdd PMOS_HP L=45n W=300n

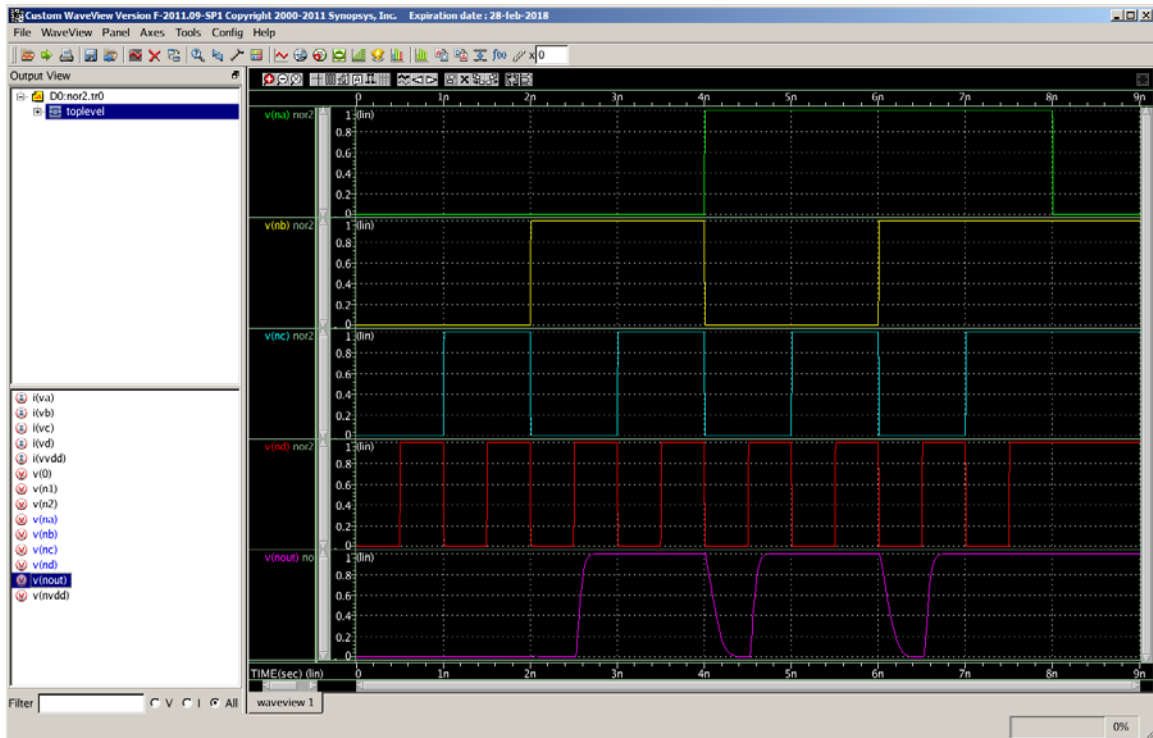mp2 n1 npB npVdd npVdd PMOS_HP L=45n W=300n

.ends myNor2

* Subckt instantiation (see the port mapping. The order should match the order of the
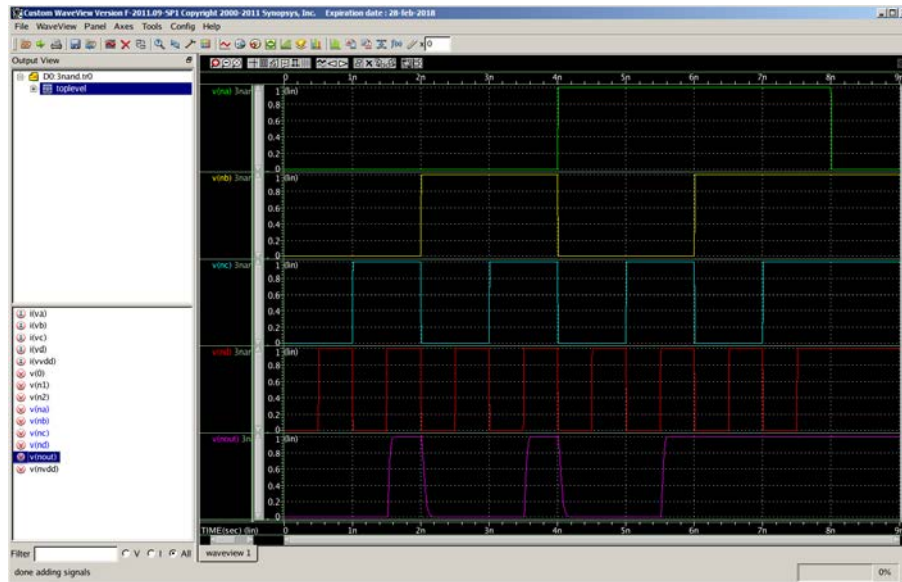* port definition of the subckt.
X1 nA nB n1 nVdd 0 myNor2
X2 nC nD n2 nVdd 0 myNor2
X3 n1 n2 nOut nVdd 0 myNor2

- The following shows a sample waveform for $Y = A \cdot B + C \cdot D$.

[**Submit**] Zip the HSpice netlist for Problem 3 and all the waveforms into "hw03_your_id#.zip" (e.g., hw03_012345678.zip) and submit it by email.