Homework Assignment 7
(Due 4:10pm, Feb. 9, email to daehyun@eecs.wsu.edu)

(1) **[Process Variation, 20 points]** A fabrication process has several uncontrollable process variation sources, so the length or the width of a transistor has some variations. To simulate the variation, we will assume that each variation follows the Gaussian (normal) distribution function. First, download "hw07.zip" from the class website. Unzip it and you will see inv.sp and dly.pl. inv.sp is an HSpice netlist simulating an inverter with some variations. dly.pl is a Perl script to compute some statistics of the simulation result. "sweep monte = N" in the netlist tells HSpice to perform the Monte Carlo simulation N times. The width of each transistor is not a constant, rather it is defined by the "agauss" function, which is agauss(default value, variation value, sigma). Run "hspice inv.sp > inv.out" to perform the Monte Carlo simulation (N=100) and dump the output messages into the file "inv.out". Once the simulation is done, you will see "***** hspice job concluded".

Once the HSpice simulation is done, run "perl dly.pl inv.out" to parse the output file and obtain the statistics of the simulation. It will print out something like this.

\# fall delay values: # (# simulations)
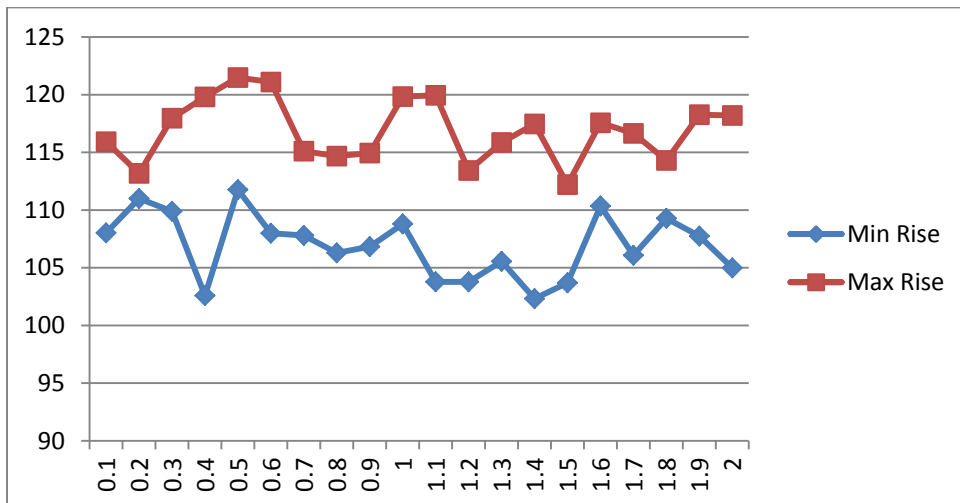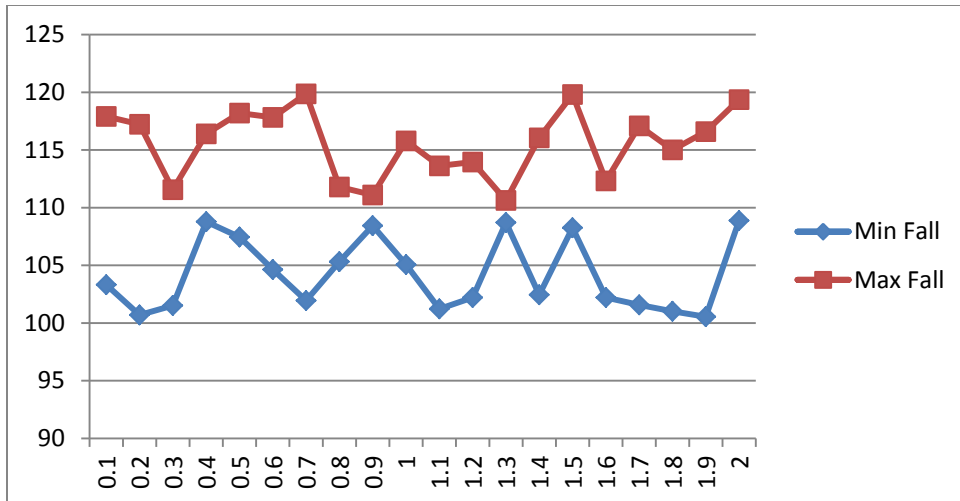
Min. fall delay

Max. fall delay

Avg. fall delay (average)

Sigma (Standard deviation)

Set the width of the PFET to 75nm (no variation) and that of the NFET to agauss (50n, Xn, 1) where X is (0.1, 0.2, …, 2.0). Simulate inv.sp for each X and find the min. fall delay and the max. fall delay for each X.

[**Submit**] Plot X vs. min. fall delay. Plot X vs. max. fall delay. Plot X vs. min. rise delay. Plot X vs max. rise delay. The following shows sample plots.

(2) **[Process Variation, 20 points]** Set the width of the NFET to 50nm (no variation) and that of the PFET to agauss (75n, Xn, 1) where X is (0.1, 0.2, …, 2.0). Simulate inv.sp for each X and find the min. fall delay and the max. fall delay for each X. [**Submit**] Plot X vs. min. fall delay. Plot X vs. max. fall delay. Plot X vs. min. rise delay. Plot X vs max. rise delay.

(3) **[Process Variation, 20 points]** Set the width of the NFET to agauss (50n, 1n, 1) and that of the PFET to 75n, run the MC simulation 10,000 times, and obtain the min fall delay (fn_min), max rise delay (fn_max), min rise delay (rn_min), and max rise delay (rn_max). Then, set the width of the NFET to 50n and that of the PFET to agauss (75n, 1n, 1), run the MC simulation 10,000 times, and obtain the

min fall delay (fp_min), max fall delay (fp_max), min rise delay (rp_min), and max rise delay (rp_max). Then, set the width of the NFET to agauss (50n, 1n, 1) and that of the PFET to agauss (75n, 1n, 1), run the MC simulation 10,000 times, and obtain the min fall delay (fnp_min), max fall delay (fnp_max), min rise delay (rnp_min), and max rise delay (rnp_max). [**Submit**] Submit the 12 min/max fall/rise delay values.

fn_min	
fn_max	
rn_min	
rn_max	
fp_min	
fp_max	
rp_min	
rp_max	
fnp_min	
fnp_max	
rnp_min	
rnp_max	

Compare the following values (use < and > symbols. for example, fn_min<fp_min<fnp_min).

(a) fn_min, fp_min, fnp_min

(b) fn_max, fp_max, fnp_max

(c) rn_min, rp_min, rnp_min

(d) rn_max, rp_max, rnp_max