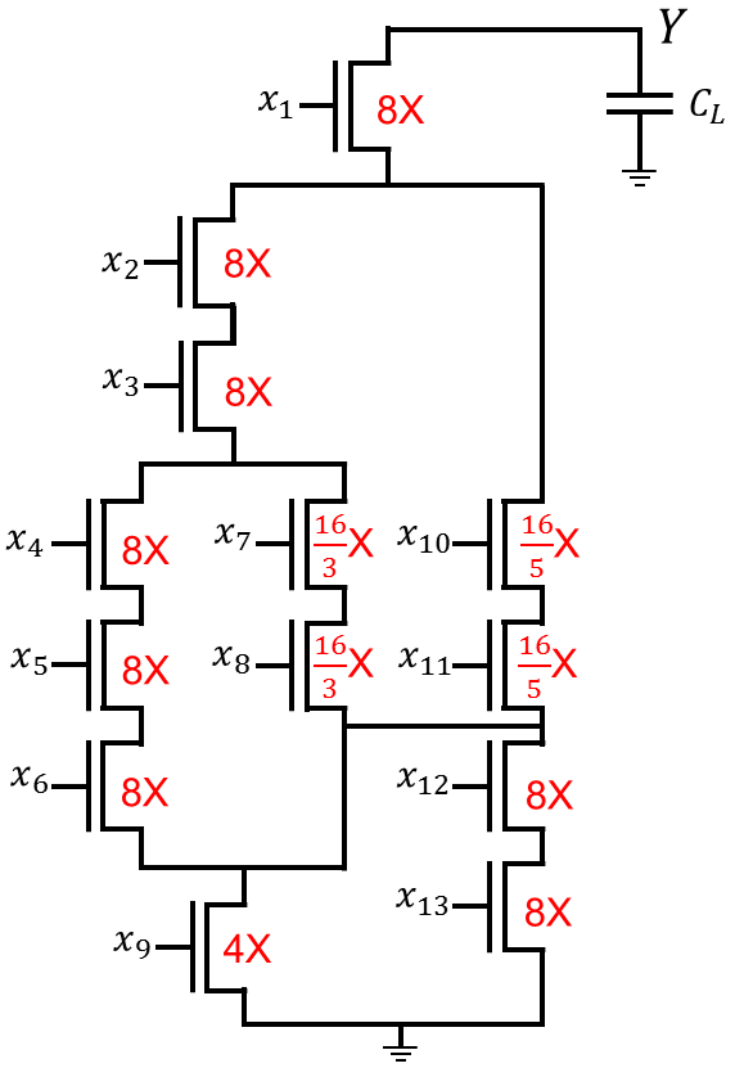
Homework Assignment 9
(Due 4:10pm, Feb. 14, email to daehyun@eecs.wsu.edu)

(1) **[TR Sizing, 20 points]** The following shows a schematic of the NFET network of a static CMOS gate. Size the transistors so that the fall delay is less than or equal to $R_n C_L$ where R_n is the resistance of a 1X NFET. Try to minimize the total width. Find the total width.



W=85.07X

(2) **[PDE, 10 points]** x, y, z are variables and a, b, c are constants. Find the partial derivatives of $F(x, y, z) = ax^4 + bx^2y^3z + cx^3y^2z^2 + x^2y^4$ with respect to x, y, and z.

$$\frac{\partial F}{\partial x} = 4ax^3 + 2bxy^3z + 3cx^2y^2z^2 + 2xy^4$$

$$\frac{\partial F}{\partial y} = 3bx^2y^2z + 2cx^3yz^2 + 4x^2y^3$$

$$\frac{\partial F}{\partial z} = bx^2y^3 + 2cx^3y^2z$$

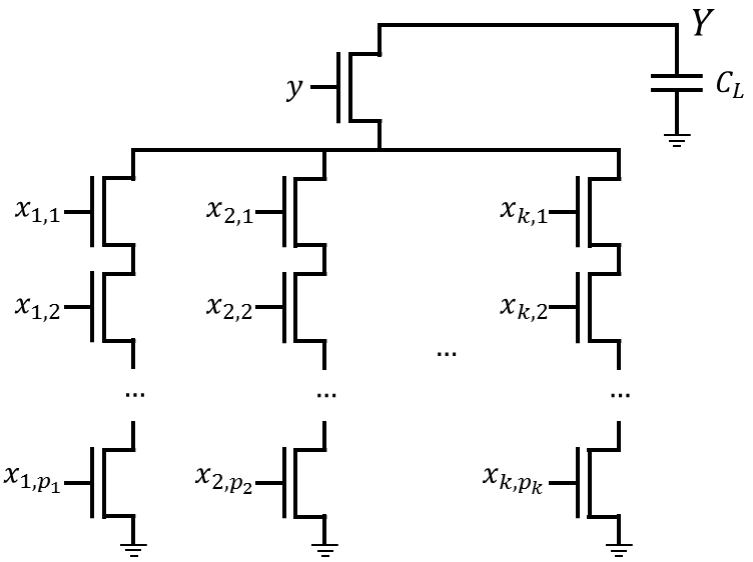
(3) [**PDE, 10 points**] x, y, z are variables. Find the partial derivatives of $G(x, y, z) = \sin(y^2 + z^2) \cdot \cos(xyz)$ with respect to x, y, and z.

$$\frac{\partial G}{\partial x} = -\sin(y^2 + z^2)\sin(xyz)\,yz$$

$$\frac{\partial G}{\partial y} = 2ycos(y^2 + z^2)\cos(xyz) - \sin(y^2 + z^2)\sin(xyz)\,xz$$

$$\frac{\partial G}{\partial z} = 2zcos(y^2 + z^2)\cos(xyz) - \sin(y^2 + z^2)\sin(xyz)\,xy$$

(4) [**Design, 20 points**] The following (in the next page) shows an NFET network of $Y = \overline{y \cdot (x_{1,1} \cdot x_{1,2} \cdot \ldots \cdot x_{1,p_1} + x_{2,1} \cdot x_{2,2} \cdot \ldots \cdot x_{2,p_2} + \cdots + x_{k,1} \cdot x_{k,2} \cdot \ldots \cdot x_{k,p_k})} = \overline{y \cdot \sum_{i=1}^{k} \prod_{j=1}^{p_k} x_{i,j}}$ (Notice that k, $p_1, \ldots, p_k$ are constants). Size the transistors so that the fall delay is less than or equal to R_nC_L where R_n is the resistance of a 1X NFET. Minimize the total width. Find the total width.



The width of $x_{i,j}$: w_i

The width of y: Y

Timing constraint for each path: $\frac{1}{Y} + \sum_{j=1}^{p_i} \frac{1}{w_{i,j}} = \frac{1}{Y} + \frac{p_i}{w_i} = 1$ (for $i = 1, \dots, k$)

From the constraint: $w_i = \frac{p_i \cdot Y}{Y-1}$

Total width $W = Y + \sum p_i w_i = Y + \frac{Y}{Y-1} \cdot \sum {p_i}^2 = Y + \frac{sY}{Y-1}$ where $s = \sum {p_i}^2$

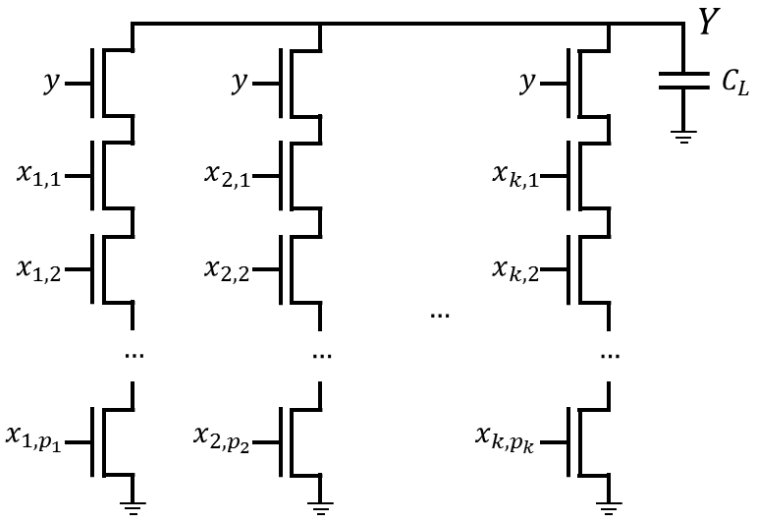
$\frac{dW}{dY} = 1 + s\frac{(Y-1)-Y}{(Y-1)^2} = 1 - \frac{s}{(Y-1)^2} = 0$, so $Y = 1 + \sqrt{s}$

$$\therefore Y = 1 + \sqrt{{p_1}^2 + {p_2}^2 + \cdots + {p_k}^2}$$

$$w_i = p_i \cdot \left(1 + \frac{1}{\sqrt{{p_1}^2 + {p_2}^2 + \cdots + {p_k}^2}}\right)$$

$$W = \left(1 + \sqrt{{p_1}^2 + {p_2}^2 + \cdots + {p_k}^2}\right)^2$$

(5) [**Design, 20 points**] The following (in the next page) shows an NFET network of Y in Problem 4. Size the transistors so that the fall delay is less than or equal to $R_n C_L$ where R_n is the resistance of a 1X NFET. Minimize the total width. Find the total width.



The width of the transistors in the i-th column: w_i

Timing constraint for the i-th column: $\frac{p_i+1}{w_i} = 1$

Thus, $w_i = p_i + 1$

Total width: $\sum(p_i + 1) \cdot w_i = \sum(p_i + 1)^2$

(6) [**Math, 10 points**] Compare the total widths you found in Problem 4 and Problem 5. Which implementation is better (occupy smaller area)?

The design in Problem 4 is better.

$$W_{problem5} - W_{problem4} = \sum(p_i + 1)^2 - \left(1 + \sqrt{{p_1}^2 + {p_2}^2 + \cdots + {p_k}^2}\right)^2$$

$$= \left\{\sum {p_i}^2 + 2\sum p_i + k\right\} - \left\{\sum {p_i}^2 + 2\sqrt{{p_1}^2 + {p_2}^2 + \cdots + {p_k}^2} + 1\right\}$$

$$= 2\left(\sum p_i - \sqrt{{p_1}^2 + {p_2}^2 + \cdots + {p_k}^2}\right) + (k - 1)$$

The first term is positive because $(\sum p_i)^2 - \left(\sqrt{{p_1}^2 + {p_2}^2 + \cdots + {p_k}^2}\right)^2 = 2\sum_{i,j,i\neq j} p_i p_j > 0$. The second term is also positive or zero because $k \geq 1$.

Thus, $W_{problem5} - W_{problem4} > 0$.