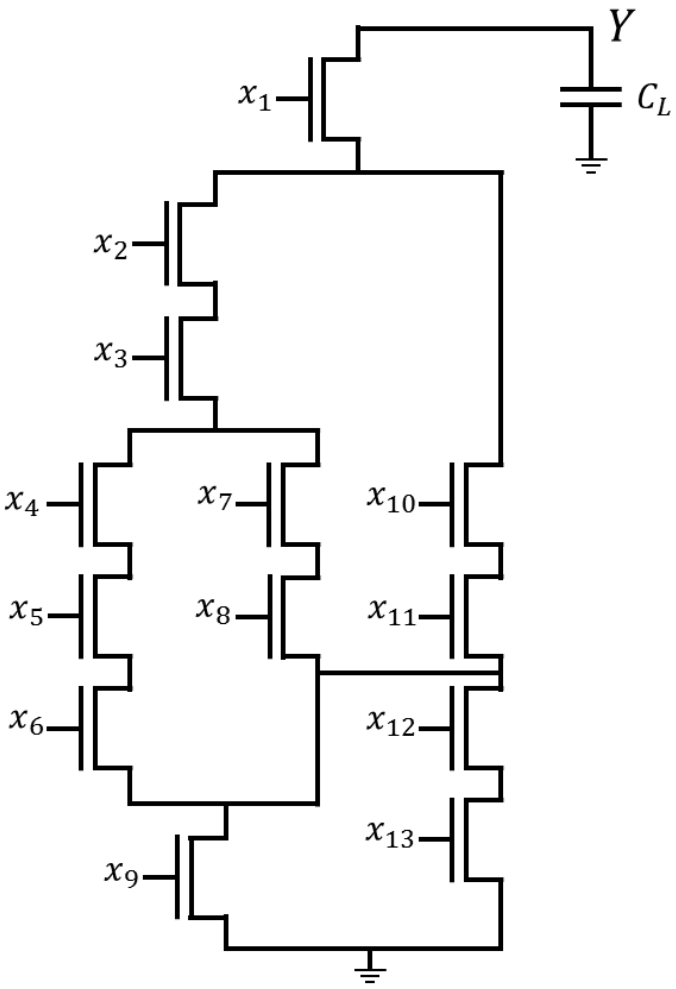
Homework Assignment 9
(Due 4:10pm, Feb. 14, email to daehyun@eecs.wsu.edu)

(1) **[TR Sizing, 20 points]** The following shows a schematic of the NFET network of a static CMOS gate. Size the transistors so that the fall delay is less than or equal to $R_n C_L$ where R_n is the resistance of a 1X NFET. Try to minimize the total width. Find the total width.



(2) **[PDE, 10 points]** x, y, z are variables and a, b, c are constants. Find the partial derivatives of $F(x, y, z) = ax^4 + bx^2y^3z + cx^3y^2z^2 + x^2y^4$ with respect to x, y, and z.

$\frac{\partial F}{\partial x} =$

$\frac{\partial F}{\partial y} =$

$\frac{\partial F}{\partial z} =$

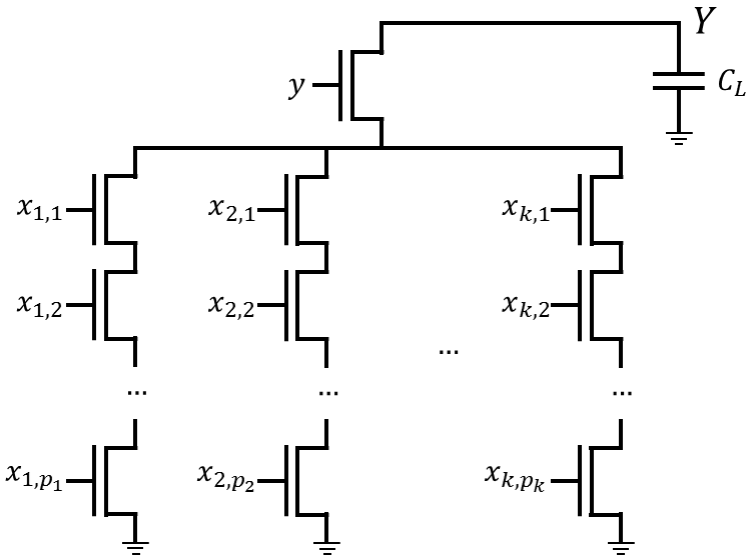
(3) [**PDE, 10 points**] x, y, z are variables. Find the partial derivatives of $G(x, y, z) = \sin(y^2 + z^2) \cdot \cos(xyz)$ with respect to x, y, and z.

$\frac{\partial G}{\partial x} =$

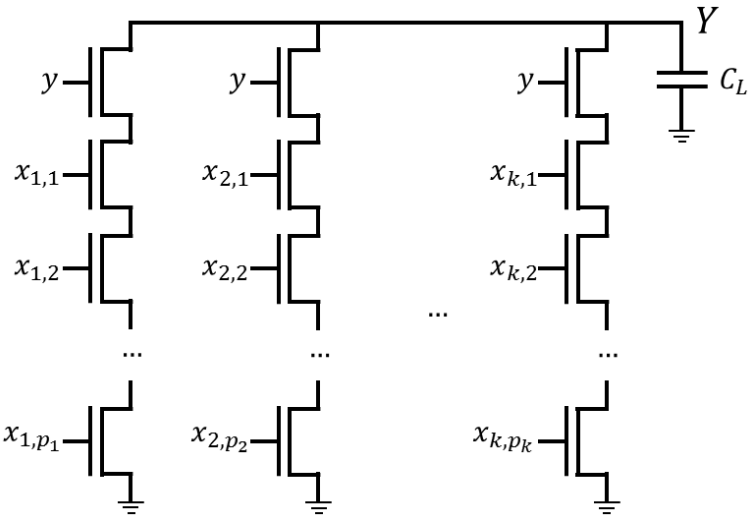
$\frac{\partial G}{\partial y} =$

$\frac{\partial G}{\partial z} =$

(4) [**Design, 20 points**] The following (in the next page) shows an NFET network of $Y = \overline{y \cdot (x_{1,1} \cdot x_{1,2} \cdot \ldots \cdot x_{1,p_1} + x_{2,1} \cdot x_{2,2} \cdot \ldots \cdot x_{2,p_2} + \cdots + x_{k,1} \cdot x_{k,2} \cdot \ldots \cdot x_{k,p_k})} = \overline{y \cdot \sum_{i=1}^{k} \prod_{j=1}^{p_k} x_{i,j}}$ (Notice that k, $p_1, \ldots, p_k$ are constants). Size the transistors so that the fall delay is less than or equal to $R_n C_L$ where R_n is the resistance of a 1X NFET. Minimize the total width. Find the total width.



(5) [**Design, 20 points**] The following (in the next page) shows an NFET network of Y in Problem 4. Size the transistors so that the fall delay is less than or equal to $R_n C_L$ where R_n is the resistance of a 1X NFET. Minimize the total width. Find the total width.



(6) [**Math, 10 points**] Compare the total widths you found in Problem 4 and Problem 5. Which implementation is better (occupy smaller area)?