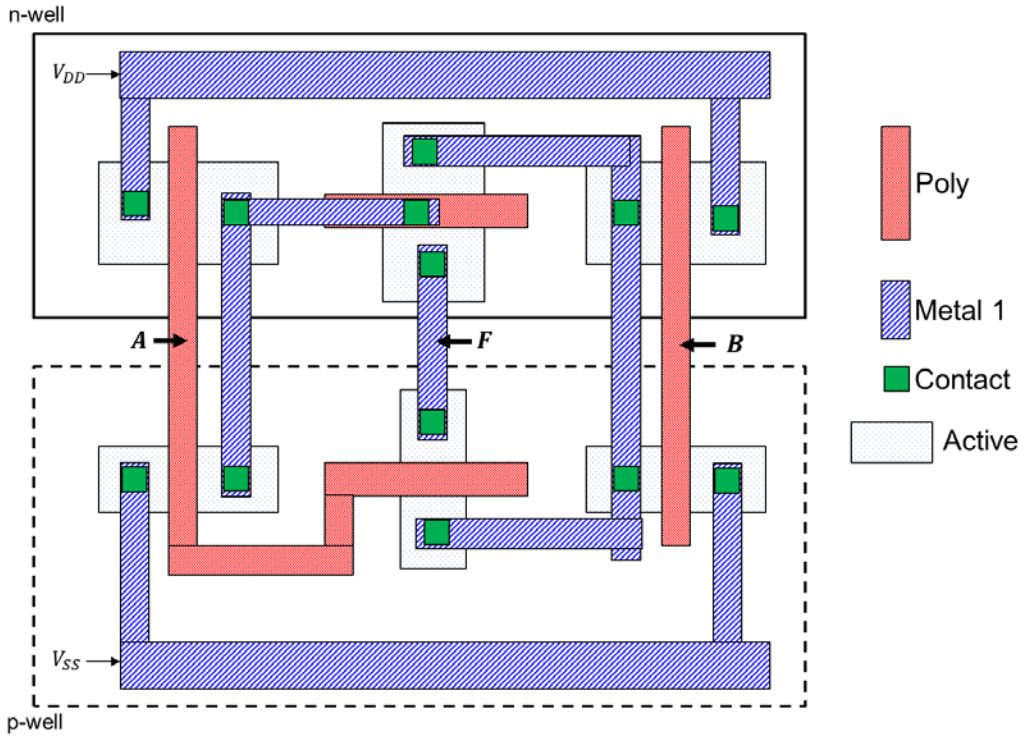
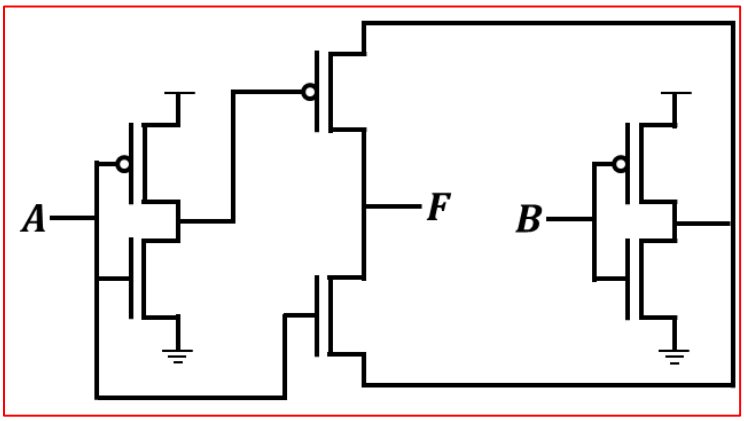
Homework Assignment 10
(Due 4:10pm, Mar. 5, email to daehyun@eecs.wsu.edu)

(1) **[Layout, 20 points]** Convert the following layout into a transistor-level schematic. Input: A, B. Output: F.





(2) **[Layout, 20 points]** Convert the following layout into a transistor-level schematic. Input: A, B, C. Output: F.