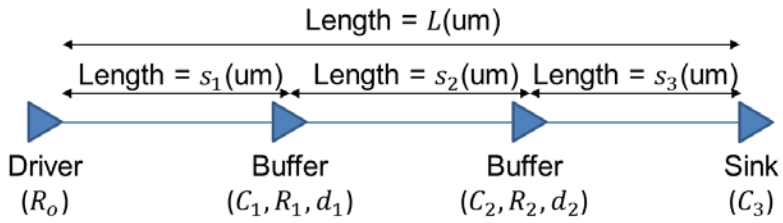
Homework Assignment 16
(Due 4:10pm, Apr. 18, email to daehyun@eecs.wsu.edu)

(1) **[Interconnect, 30 points]** Find the locations (s_1 and s_2) of the two buffers minimizing the total delay (i.e., express s_1 and s_2 as functions of $L, R_0, R_1, R_2, C_1, C_2, C_3, r, c$).



- R_0: Output resistance of the driver
- R_1, R_2: Output resistances of the first and second buffers, respectively
- C_1, C_2: Input capacitances of the first and second buffers, respectively
- C_3: Input capacitance of the sink
- r, c: Unit wire resistance (ohm/um) and capacitance (F/um), respectively
- d_1, d_2: Delays of the first and second buffers, respectively
- L: Total wire length