# Lab 1
# (Due 23:59, Apr. 20th)

Draw a layout for a full adder (primary inputs: A, B, CI, primary outputs: S, CO). Do not use the Metal 2 to Metal 10 layers. Run DRC, LVS, and PEX. Once you get a netlist with parasitic RC, run HSpice to obtain rise and fall delay values. You need to create proper input waveforms to test the rise and fall delays at S and CO. The following shows some specifications you should satisfy:

- Load capacitance: 10fF
- Worst-case delay for the given load cap: 200ps
- Die area $\leq$ 5um X 2.5um

**Tips**

- Draw a schematic first and properly size the transistors.
- Run HSpice simulation.
- Draw a layout and run DRC, LVS, PEX.
- Refer to the FA schematic shown in the lecture notes.

**Submit**

- Layout snapshot
- Transistor-level schematic (with the size of each transistor)
- DRC, LVS, PEX reports
    - Do not print them out. You can just zip the report files and send it to me by email).
- Input and output waveforms (use WaveView).
- The worst-case rise and fall delays at S and CO.