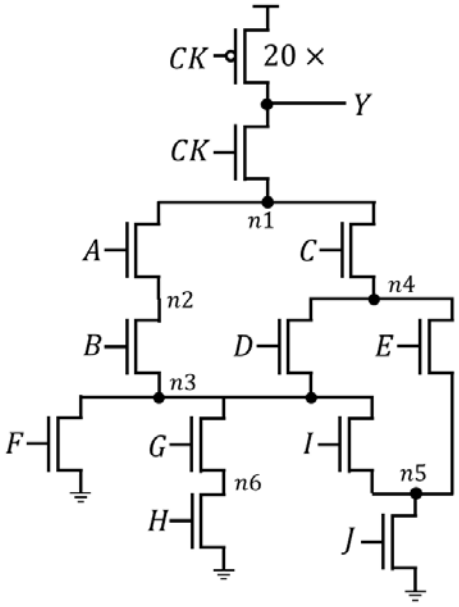
Lab 2
(Due 23:59, Mar. 29th)

Size the NFETs in the following dynamic-CMOS circuit.



- Download http://eecs.wsu.edu/~ee434/Labs/lab2.zip and unzip it. There is lab2.sp. Use the netlist. You can change the widths of the NFETs in the netlist.
- Do not touch anything else except the widths of the NFETs.
- The width of a 1X transistor is 50nm.
- The width of each NFET should be an integer multiple of 50nm. For example, you can use 100nm (2X), 250nm (5X), etc., but you cannot use 67nm, 271nm, etc.
- Objective: Minimize the total width of the NFETs.
- Constraint: For each path, the fall delay should be less than or equal to 60ps.
- Use HSpice to simulate it.
- What to submit
    - Final netlist.

Grading criteria

- If all the paths satisfy the timing constraint:
    - Total area (A) <= 10,500nm: 100 points
    - 10,500nm < A <= 10,550nm: 95 points

- 10,550nm < A <= 10,600nm: 90 points
- etc.

- If some of the paths do not satisfy the timing constraint:
  - A <= 10,500nm: 100 points – 2*$\sum(Delay - 60ps)$ (Sum is for all the violating paths)
  - 10,500nm < A <= 10,550nm: 95 points – 2*$\sum(Delay - 60ps)$
  - etc.