Lab 2
(Due Apr. 20th (Friday), 11:59:59pm)

Design a dual-edge D flip-flop (i.e., it captures the input signal at both rising and falling clock edges).

Specification

- Data input: D
- Clock input: CK
- Output: Q
- It has a synchronous active-high set input (S).
- It has a synchronous active-low reset input (R).
- S dominates R, i.e., if S=1, Q=1. If S=0 and R=0, Q=0. If S=0 and R=1, it is just a dual-edge D-F/F.
- (Hint) Use the schematic in Problem 5 in the following PDF.
    - http://www.eecs.wsu.edu/~ee434/Exam/ee434-2017sm1.pdf

How to proceed

1) Draw a schematic on a paper.
2) Make an HSpice netlist.
3) Simulate it. Use the following input vectors:

VD nD 0 PWL 0p 0 250p 0 260p Vsup 1.25n Vsup 1.26n 0 2.25n 0 2.26n Vsup 3.25n Vsup 3.26n 0
VS nS 0 PWL 0p 0
VR nR 0 PWL 0p Vsup
VCK nCK 0 PWL 0p 0 10p Vsup 500p Vsup 510p 0 1n 0 1.01n Vsup 1.5n Vsup 1.51n 0 2n 0 2.01n Vsup 2.5n Vsup 2.51n 0 3n 0 3.01n Vsup 3.5n Vsup 3.51n 0

VD, VS, VR, and VCK are D, S, R, and CK, respectively.

4) **Simulation 1:** Set S=1 and R=0 (Don't touch D and CK). Run HSpice. Q should be constant logic 1 (it might have some small glitches, which is ok).
5) **Simulation 2:** Set S=1 and R=1 (Don't touch D and CK). Run HSpice. Q should be constant logic 1.

6) **Simulation 3:** Set S=0 and R=0 (Don't touch D and CK). Run HSpice. Q should be constant logic 0.
7) **Simulation 4:** Set S=0 and R=1 (Don't touch D and CK). Run HSpice. Now it should be a normal dual-edge D-F/F.

Submit

- Your HSpice netlist.
- Waveform screenshots (show D, S, R, CK, and Q) for
    - Simulation 1
    - Simulation 2
    - Simulation 3
    - Simulation 4