EE434
ASIC & Digital Systems

Active-HDL

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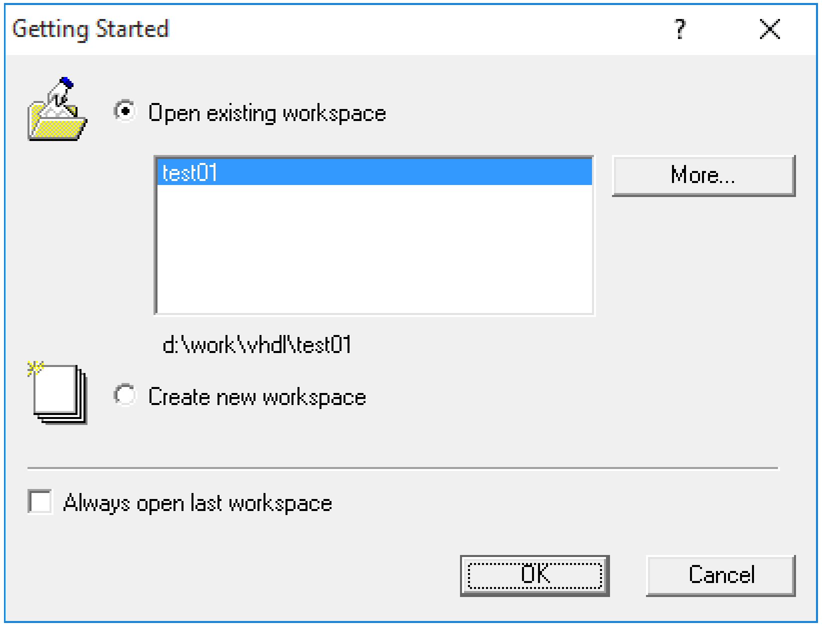
Download

- http://www.aldec.com
  - PRODUCTS → Active-HDL → Free Evaluation
    - (requires registration)

How to Run Active-HDL

- Run your Active-HDL and you will see the following screen.



Getting Started

● Open existing workspace

test01

d:\work\vhdl\test01

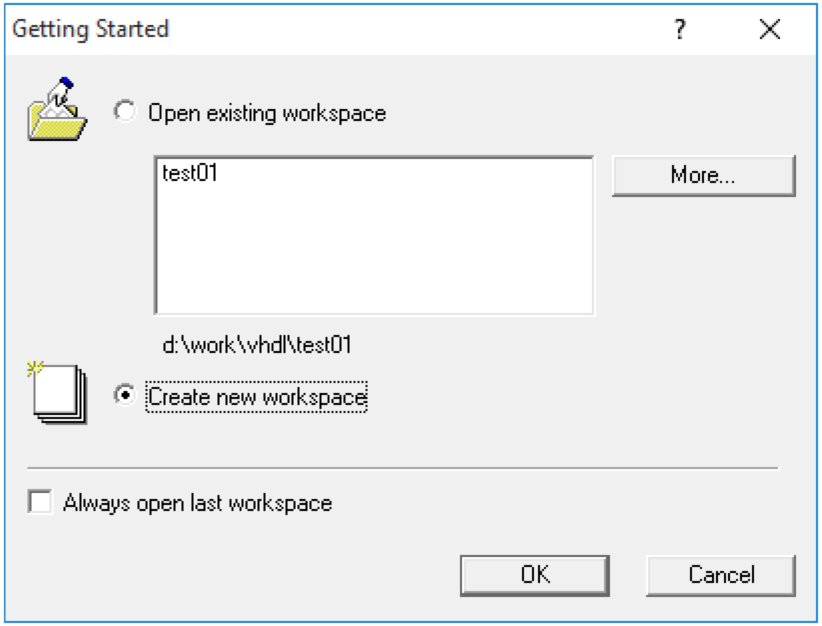
○ Create new workspace

□ Always open last workspace

How to Run Active-HDL

- If you want to open an existing workspace, select it and click OK.

- If you want to create a new workspace, select “Create new workspace” and click OK.



Getting Started

○ Open existing workspace

test01

d:\work\vhdl\test01

● Create new workspace

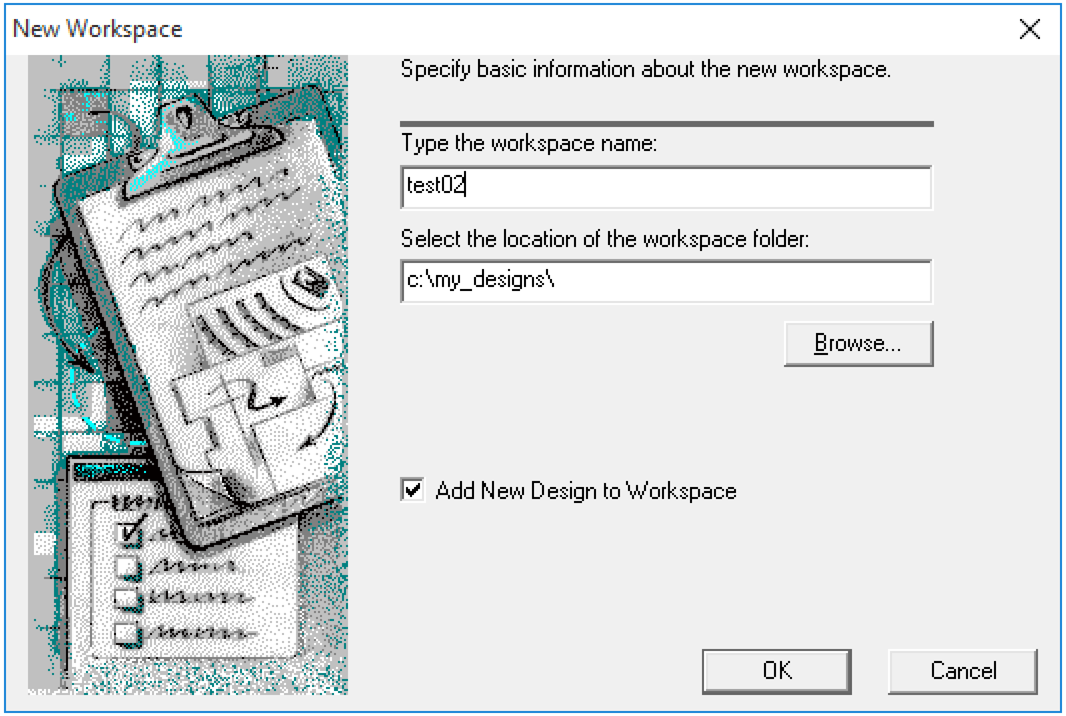
□ Always open last workspace

Create a New Workspace

- Type the workspace name.

- Turn on “Add New Design to Workspace.

- Click OK.



New Workspace

Specify basic information about the new workspace.

Type the workspace name:

test02

Select the location of the workspace folder:

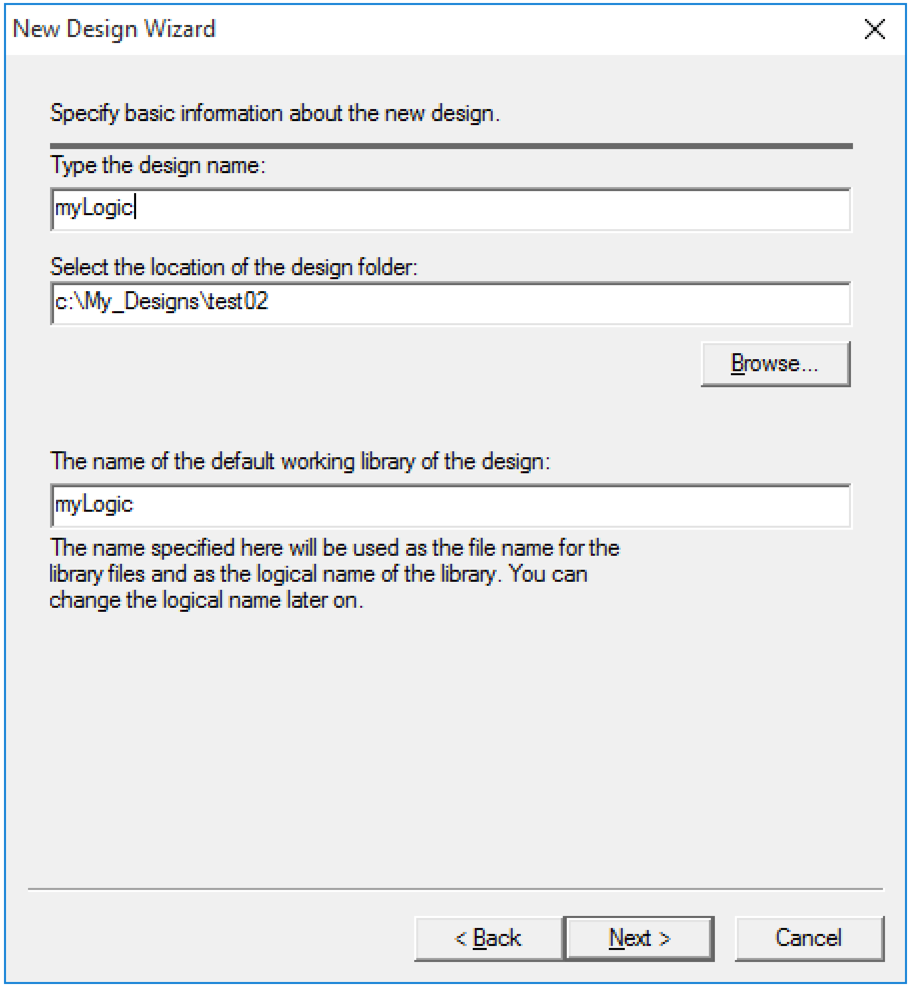
c:\my_designs\

☑ Add New Design to Workspace

Create a New Workspace

- In the “New Design Wizard” window, select “Create an Empty Design” and click Next.
- If you see a “Property Page” window, just click Next.
- In the “New Design Wizard” window, type a design name and click Next (see the next slide).

Create a New Workspace



Specify basic information about the new design.

Type the design name:

myLogic

Select the location of the design folder:

c:\My_Designs\test02

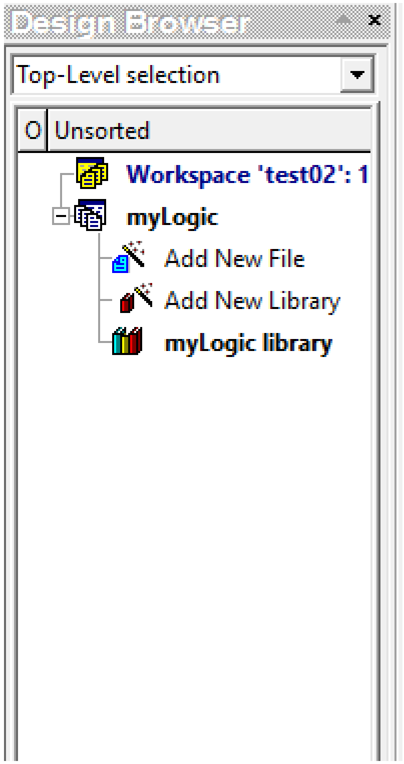
The name of the default working library of the design:

myLogic

The name specified here will be used as the file name for the library files and as the logical name of the library. You can change the logical name later on.

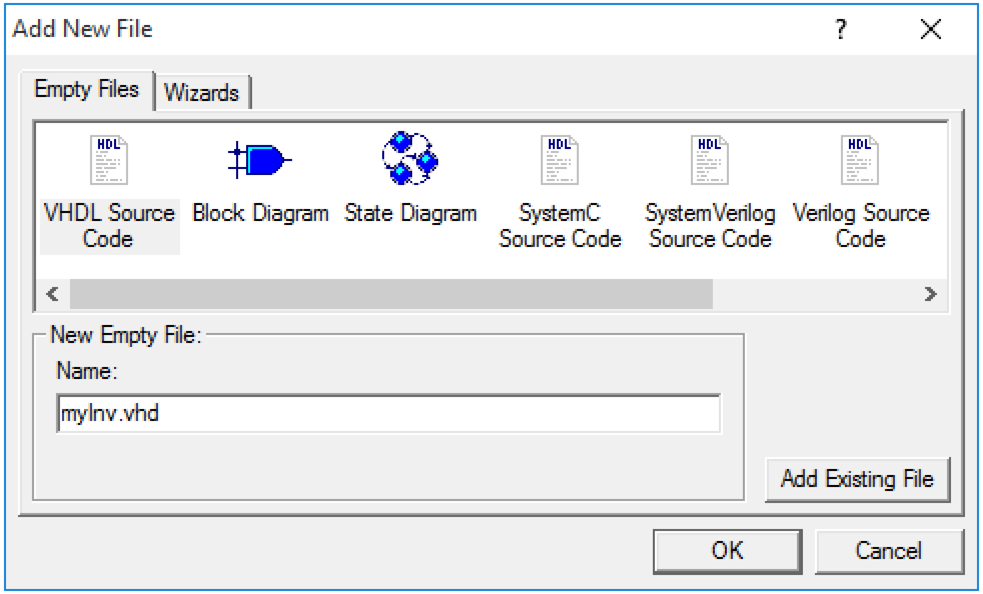
Design Browser

- You will see a design browser window in the left.



Add a New File to the Design

- Click File → New → VHDL Source.
- Or double-click “Add New File” in the design browser to add a new file to the existing design.
- I am creating and adding “myInv.vhd” to my design.

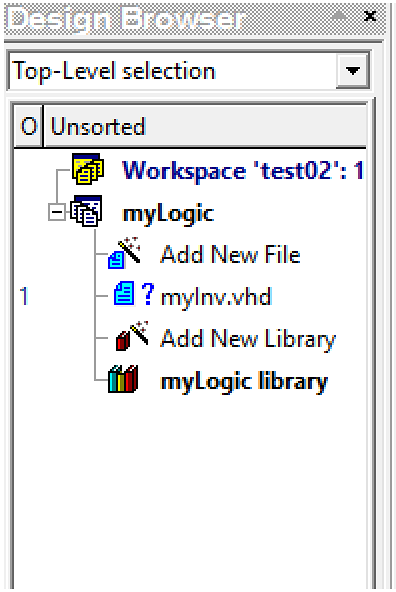


New Empty File:

Name: myInv.vhd

Add a New File to the Design

- I successfully created and added “myInv.vhd” to myLogic.
- The ? Symbol in front of the file name means that it’s not been compiled.



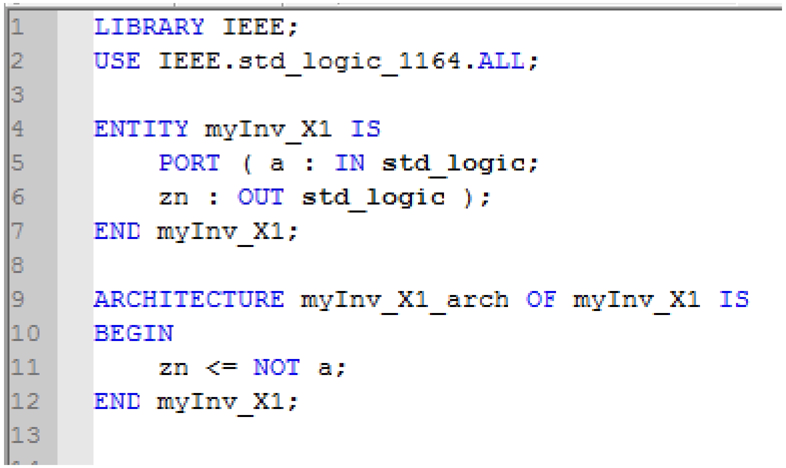
Design Browser

Top-Level selection

O	Unsorted
	Workspace 'test02': 1
	myLogic
	Add New File
1	? myInv.vhd
	Add New Library
	myLogic library

Edit and Compile

- Add the following code to myinv.vhd.

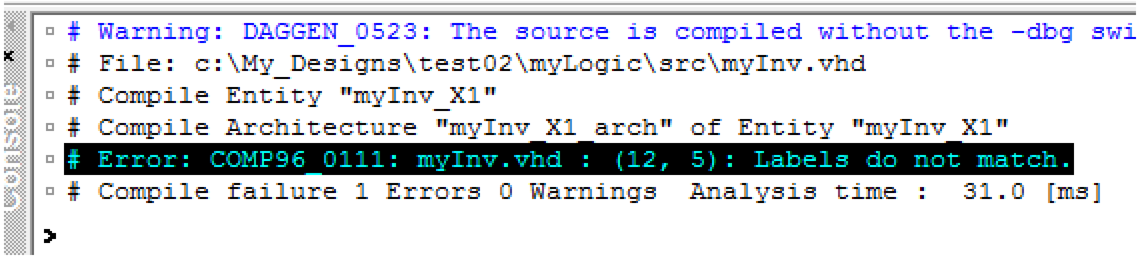


```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

ENTITY myInv_X1 IS
    PORT ( a : IN std_logic;
    zn : OUT std_logic );
END myInv_X1;

ARCHITECTURE myInv_X1_arch OF myInv_X1 IS
BEGIN
    zn <= NOT a;
END myInv_X1;
```

- Save and compile.
  - To compile the design, click Design → Compile or click the compile icon.

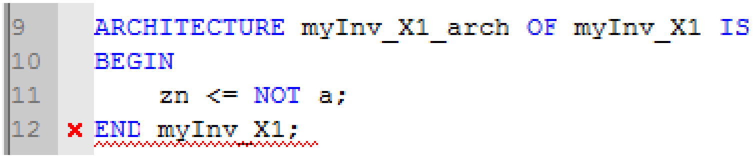
System Messages

- In the bottom of the Active-HDL window, you will see an error message as follows:



```
# Warning: DAGGEN_0523: The source is compiled without the -dbg swi
# File: c:\My_Designs\test02\myLogic\src\myInv.vhd
# Compile Entity "myInv_X1"
# Compile Architecture "myInv_X1_arch" of Entity "myInv_X1"
# Error: COMP96_0111: myInv.vhd : (12, 5): Labels do not match.
# Compile failure 1 Errors 0 Warnings  Analysis time :  31.0 [ms]
>
```

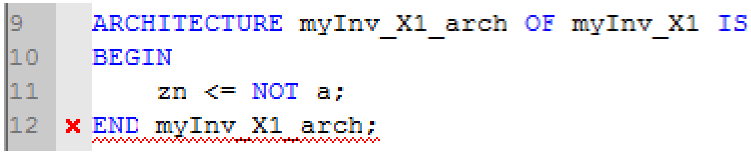
- This means that something is wrong in the 12th line, 5th character.
- Double-click the error message to directly go to the problematic line.



```
9     ARCHITECTURE myInv_X1_arch OF myInv_X1 IS
10    BEGIN
11        zn <= NOT a;
12  × END myInv_X1;
```

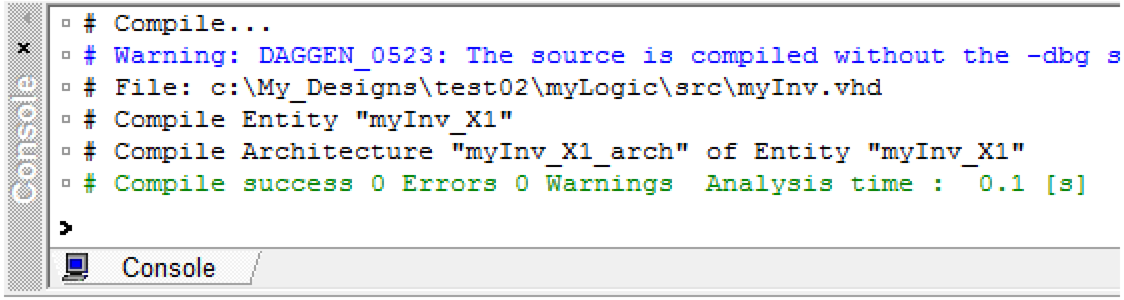
Debugging

- Fix the error as follows:



```
ARCHITECTURE myInv_X1_arch OF myInv_X1 IS
BEGIN
    zn <= NOT a;
END myInv_X1_arch;
```

- Compile the design again.

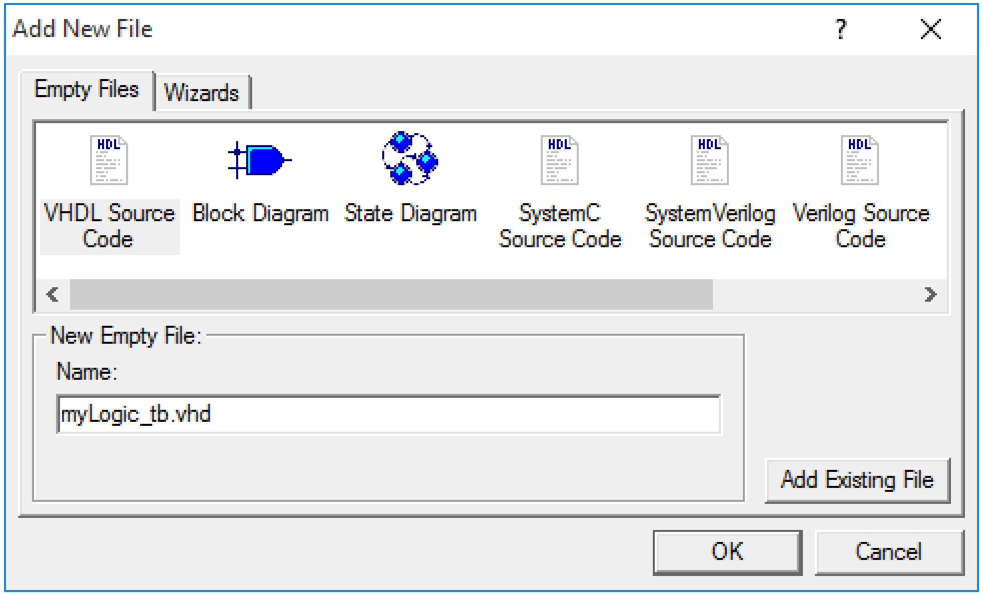


```
# Compile...
# Warning: DAGGEN_0523: The source is compiled without the -dbg s
# File: c:\My_Designs\test02\myLogic\src\myInv.vhd
# Compile Entity "myInv_X1"
# Compile Architecture "myInv_X1_arch" of Entity "myInv_X1"
# Compile success 0 Errors 0 Warnings  Analysis time :  0.1 [s]
>
```

- There is no error.

Testbench

- Double-click “Add New File” to add one more file.

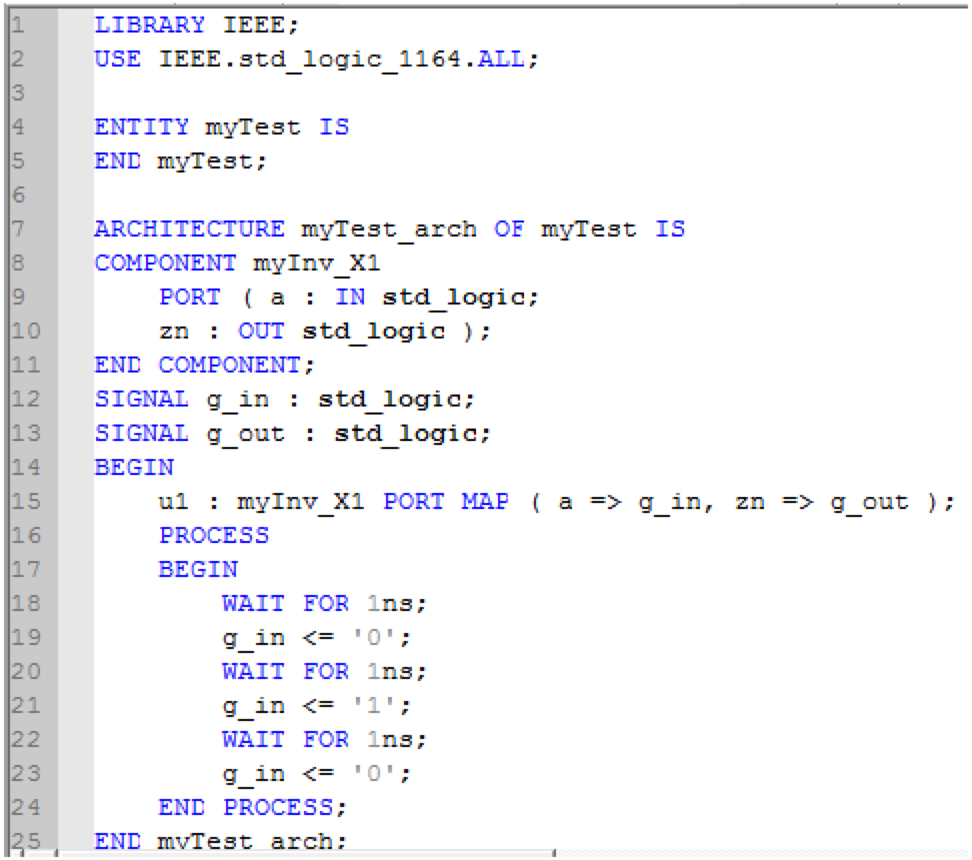


New Empty File:

Name: myLogic_tb.vhd

Testbench

- Now, I am going to test the inverter I made. To test it, I need an entity. Type the following into myLogic_tb.vhd and compile it.

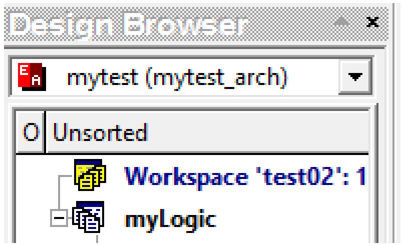


```vhdl
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

ENTITY myTest IS
END myTest;

ARCHITECTURE myTest_arch OF myTest IS
COMPONENT myInv_X1
    PORT ( a : IN std_logic;
    zn : OUT std_logic );
END COMPONENT;
SIGNAL g_in : std_logic;
SIGNAL g_out : std_logic;
BEGIN
    u1 : myInv_X1 PORT MAP ( a => g_in, zn => g_out );
    PROCESS
    BEGIN
        WAIT FOR 1ns;
        g_in <= '0';
        WAIT FOR 1ns;
        g_in <= '1';
        WAIT FOR 1ns;
        g_in <= '0';
    END PROCESS;
END myTest_arch;
```

Simulation

- First, you should choose the topmost-level module you want to run in the design browser.

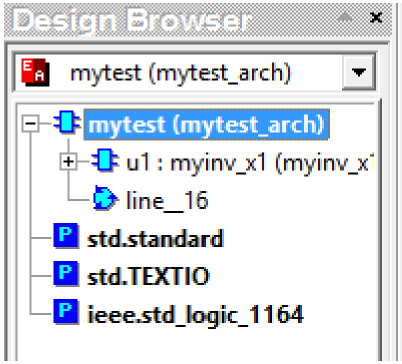
- Select myTest in the design browser as follows.



- Initialize your simulation.
  - Click Simulation → Initialize Simulation.

Simulation

- Now, you will see entities instead of files in the design browser as follows:



Design Browser

mytest (mytest_arch)

mytest (mytest_arch)

u1 : myinv_x1 (myinv_x1

line__16

std.standard

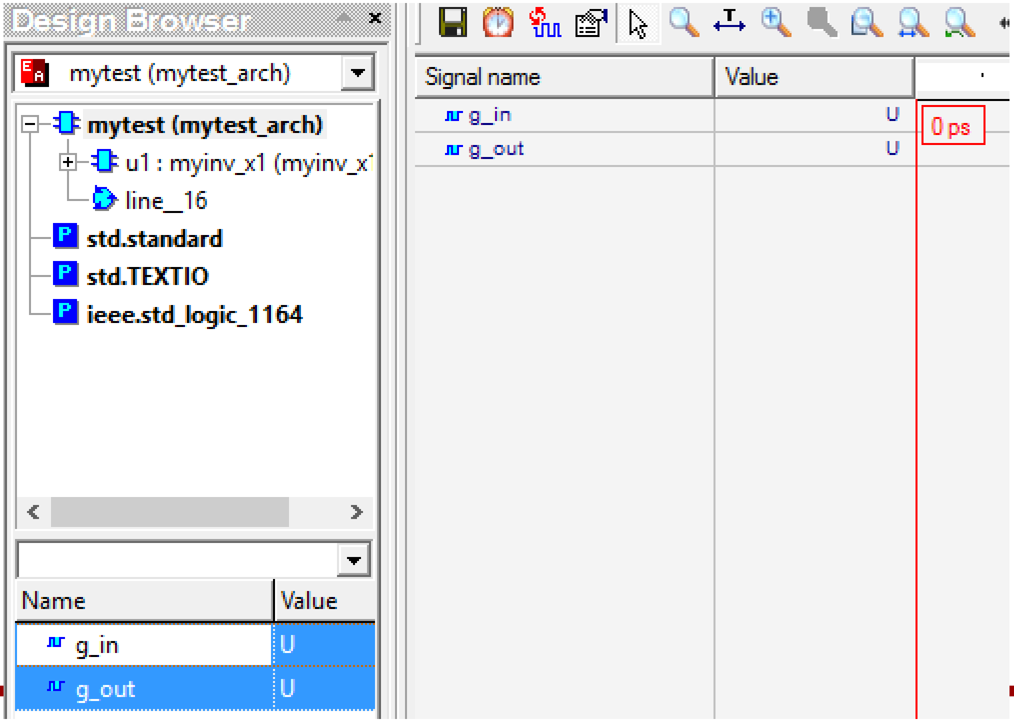
std.TEXTIO

ieee.std_logic_1164

- A simple way to check the functionality of the inverter is to look at the waveform of the output.
- Open a waveform window.
  - Click the “New waveform” icon.

Simulation

- Add the signals you want to see.
  - I want to check both the input and output.
  - Click “myTest” in the design browser and drag&drop the two signals (g_in and g_out) into the waveform window.

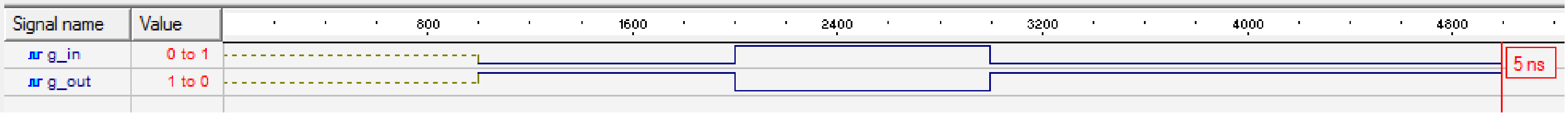


Name	Value
g_in	U
g_out	U

Signal name	Value
g_in	U
g_out	U

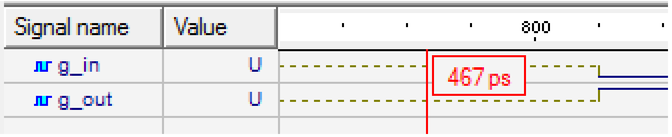
Simulation

- Simulate until 5ns.
  - Click the “Run Until” icon ⏭ and type 5ns and click OK.
- The following shows my waveform window.



Signal name	Value
g_in	0 to 1
g_out	1 to 0

- Analysis
  - Initially, the input and output are unknown (U). Click somewhere between 0 and 1ns and check their values.

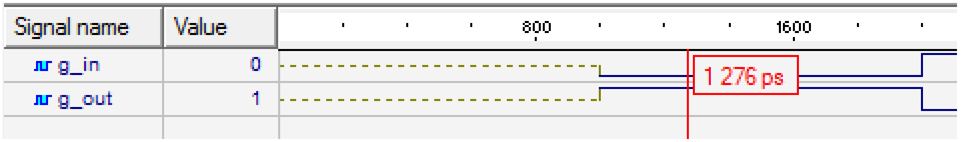


Signal name	Value
g_in	U
g_out	U

  - It is correct because we didn’t initialize the input.

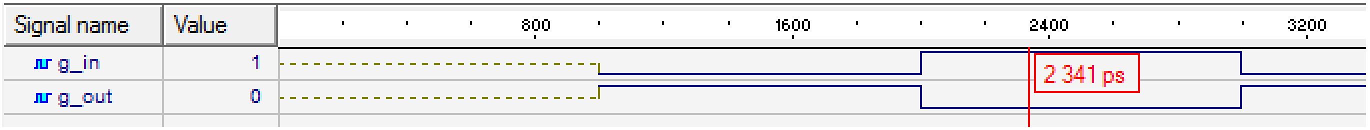
Simulation

- At 1ns, we set g_in to 0, so we get 1 at the output.



Signal name	Value
g_in	0
g_out	1

- At 2ns, we set g_in to 1, so we get 0 at the output.



Signal name	Value
g_in	1
g_out	0

Simulation

- Finish your simulation.
  - Click the “End simulation” icon. ■