EE434
ASIC & Digital Systems

ModelSim

Dae Hyun Kim
daehyun@eecs.wsu.edu

Connect to the EE434 Server

- ssh1.eecs.wsu.edu
- ssh2.eecs.wsu.edu
- ssh3.eecs.wsu.edu
- ssh4.eecs.wsu.edu

- Create a directory.
  - mkdir ee434_hdl

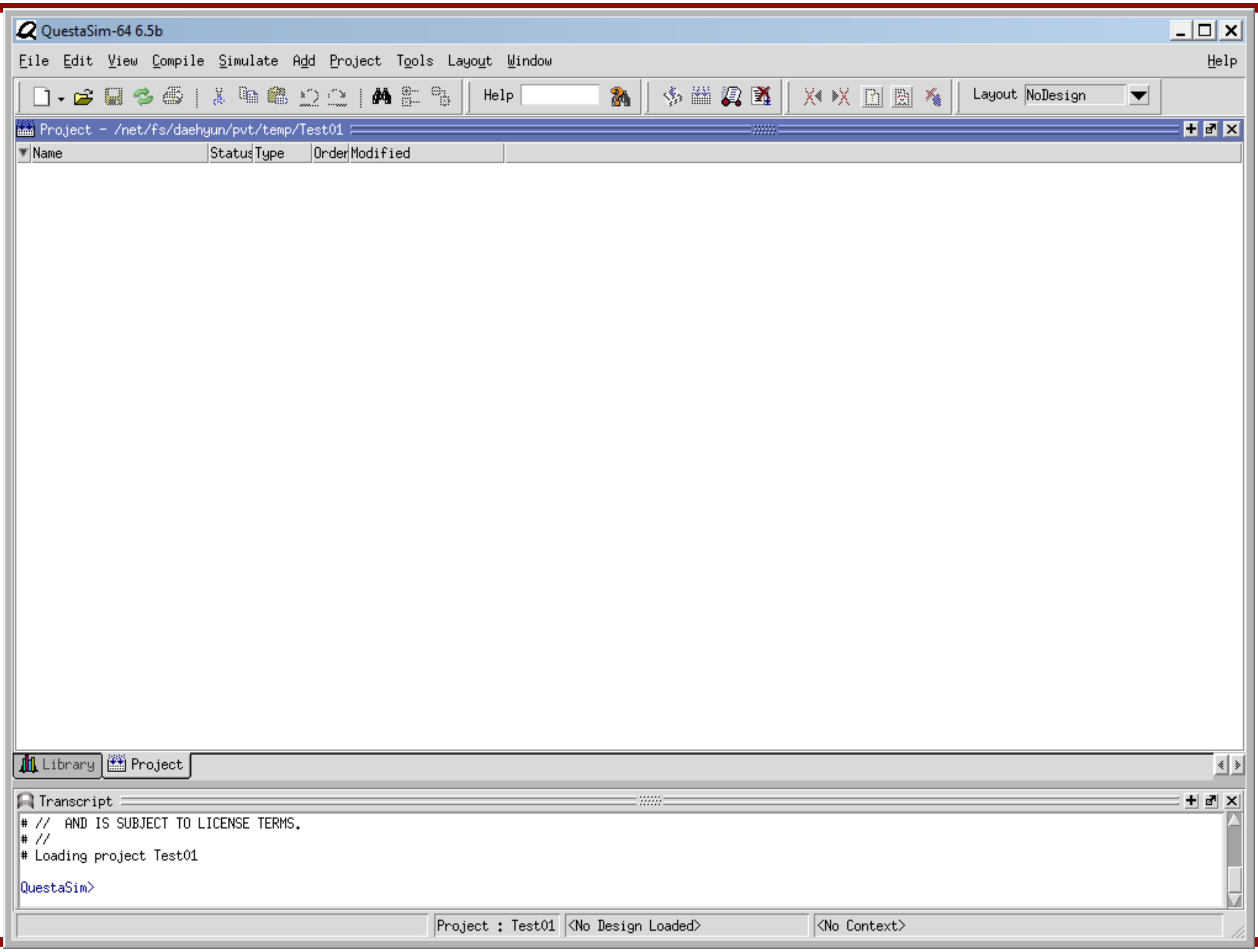
- Change to the new directory.
  - cd ee434_hdl

Run ModelSim

- Source the following file (you should source this file whenever you newly connect to the servers):
  - source /net/ictools/sh/mentor-modelsim.sh

- Run ModelSim
  - vsim

Main Window



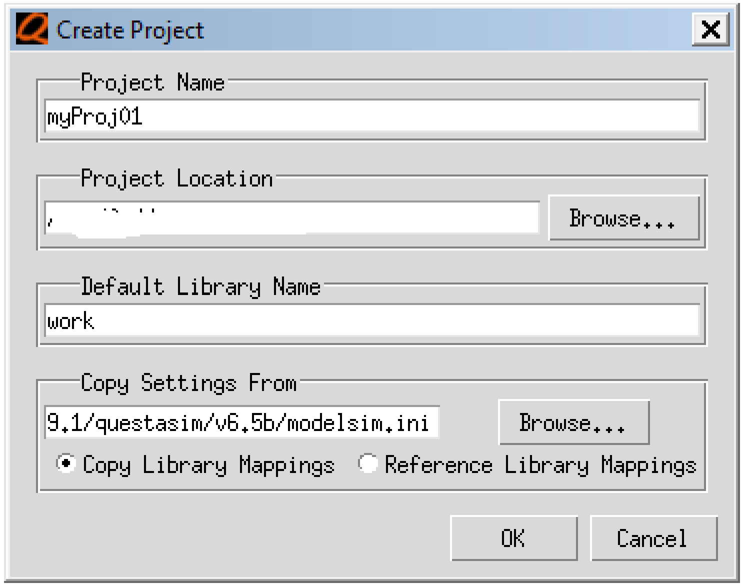
QuestaSim-64 6.5b
File Edit View Compile Simulate Add Project Tools Layout Window Help
Help
Layout NoDesign
Project - /net/fs/daehyun/pvt/temp/Test01
Name Status Type Order Modified
Library
Project
Transcript

```
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading project Test01

QuestaSim>
```

Project : Test01 <No Design Loaded> <No Context>

Create a New Project

- Click File → New → Project.



Create Project

Project Name: myProj01

Project Location: /

Default Library Name: work

Copy Settings From: 9.1/questasim/v6.5b/modelsim.ini

● Copy Library Mappings ○ Reference Library Mappings

- Enter a project name and click OK.
- If you see a “Add items to the Project” window, close it.

Project & Library

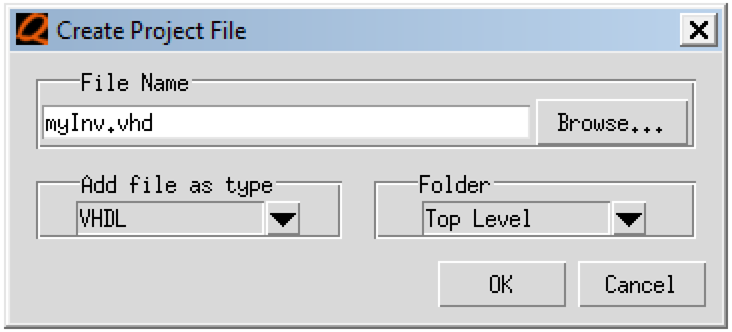
- Now, you have just made a project.

- Click the “Library” tab to see the list of libraries included in the project.

- Your work library is “work”.

Add a New File to Your Project

- Click the “Project” tab.
- Right-click → Add to Project → New File
- Enter myInv.vhd in the file name and click OK.



Create Project File

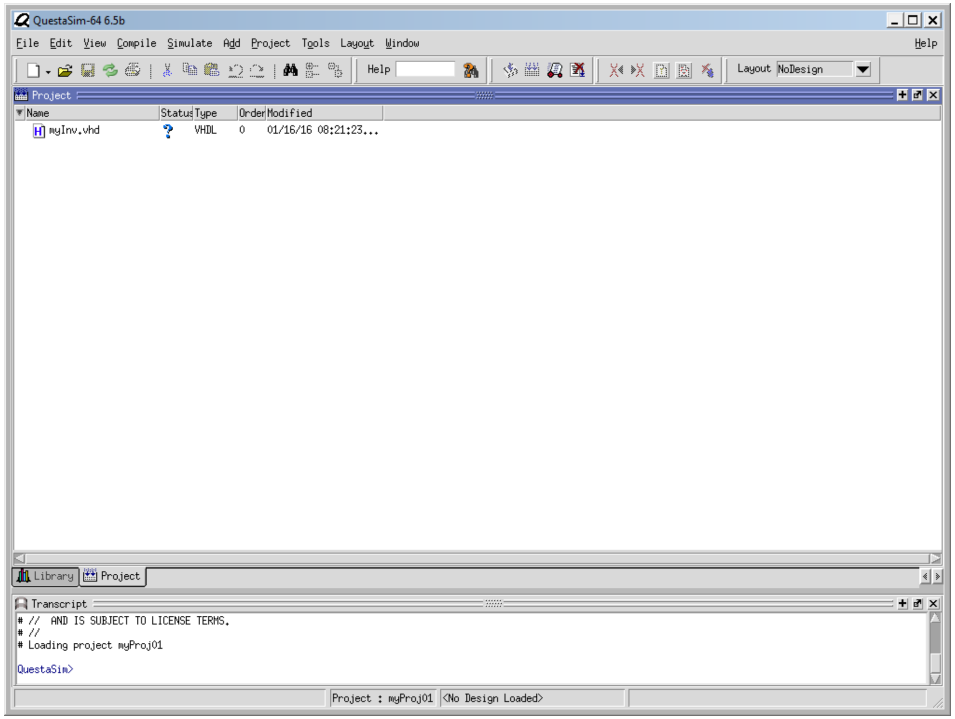
File Name: myInv.vhd

Add file as type: VHDL

Folder: Top Level

Add a New File to Your Project

- You will see the following screen.



QuestaSim-64 6.5b
File Edit View Compile Simulate Add Project Tools Layout Window Help
Help
Layout NoDesign
Project
Library
Project
Transcript

Name	Status	Type	Order	Modified
myInv.vhd	?	VHDL	0	01/16/16 08:21:23...

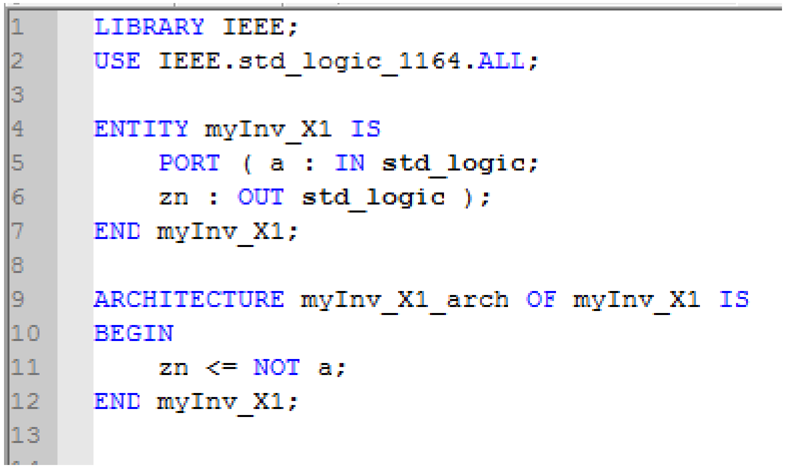
```
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading project myProj01

QuestaSim>
```

Project : myProj01 <No Design Loaded>

- Double-click myInv.vhd to open it.

Edit and Compile

- Add the following code to myInv.vhd.

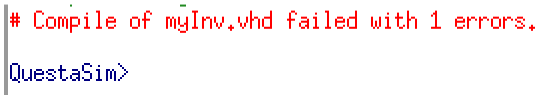


```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

ENTITY myInv_X1 IS
    PORT ( a : IN std_logic;
    zn : OUT std_logic );
END myInv_X1;

ARCHITECTURE myInv_X1_arch OF myInv_X1 IS
BEGIN
    zn <= NOT a;
END myInv_X1;
```

- Save and compile.
  - To compile the design, click Compile → Compile All or click the compile icon.

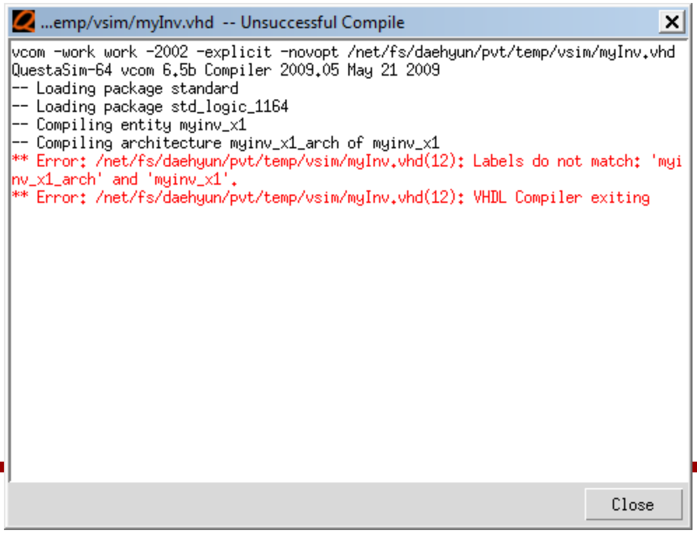
System Messages

- In the bottom of your ModelSim window, you will see an error message as follows:



```
# Compile of myInv.vhd failed with 1 errors.

QuestaSim>
```

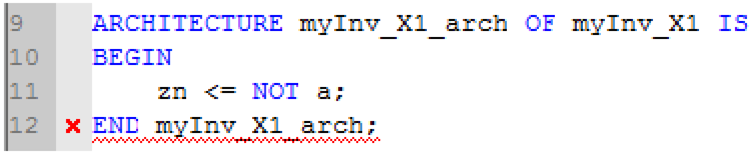
- Double-click the error message and you will see a window showing detailed error messages.
- This means that something is wrong in the 12th line.



```
vcom -work work -2002 -explicit -novopt /net/fs/daehyun/pvt/temp/vsim/myInv.vhd
QuestaSim-64 vcom 6.5b Compiler 2009.05 May 21 2009
-- Loading package standard
-- Loading package std_logic_1164
-- Compiling entity myinv_x1
-- Compiling architecture myinv_x1_arch of myinv_x1
** Error: /net/fs/daehyun/pvt/temp/vsim/myInv.vhd(12): Labels do not match: 'myi
nv_x1_arch' and 'myinv_x1'.
** Error: /net/fs/daehyun/pvt/temp/vsim/myInv.vhd(12): VHDL Compiler exiting
```

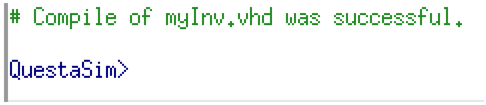
Debugging

- Fix the error as follows:



```
ARCHITECTURE myInv_X1_arch OF myInv_X1 IS
BEGIN
    zn <= NOT a;
END myInv_X1_arch;
```

- Compile the design again.

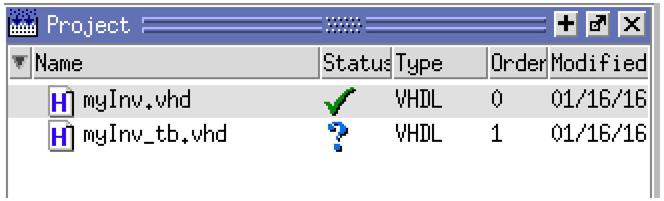


```
# Compile of myInv.vhd was successful.

QuestaSim>
```

- There is no error.

Testbench

- In the project window, add a new file named “myInv_tb.vhd”.

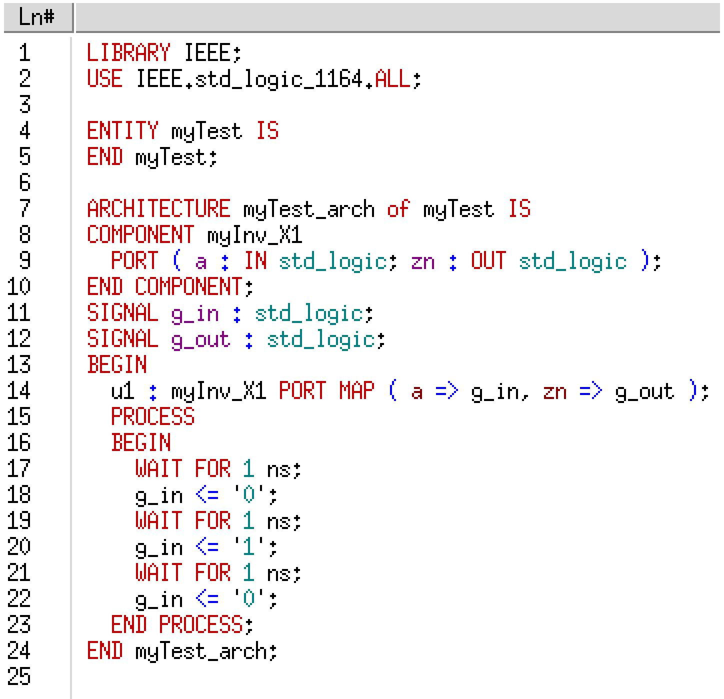


Name	Status	Type	Order	Modified
myInv.vhd	✓	VHDL	0	01/16/16
myInv_tb.vhd	?	VHDL	1	01/16/16

- The “V” symbol means that it’s been compiled correctly.

Testbench

- Now, I am going to test the inverter I made. To test it, I need an entity. Type the following into myLogic_tb.vhd and compile it.

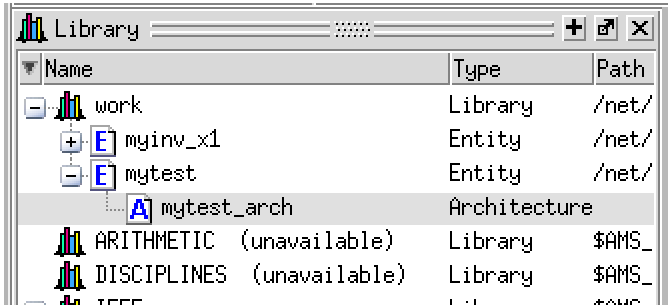


```vhdl
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

ENTITY myTest IS
END myTest;

ARCHITECTURE myTest_arch of myTest IS
COMPONENT myInv_X1
  PORT ( a : IN std_logic; zn : OUT std_logic );
END COMPONENT;
SIGNAL g_in : std_logic;
SIGNAL g_out : std_logic;
BEGIN
  u1 : myInv_X1 PORT MAP ( a => g_in, zn => g_out );
  PROCESS
  BEGIN
    WAIT FOR 1 ns;
    g_in <= '0';
    WAIT FOR 1 ns;
    g_in <= '1';
    WAIT FOR 1 ns;
    g_in <= '0';
  END PROCESS;
END myTest_arch;

```

Simulation

- Click the Library tab.

- Expand the “work” library.

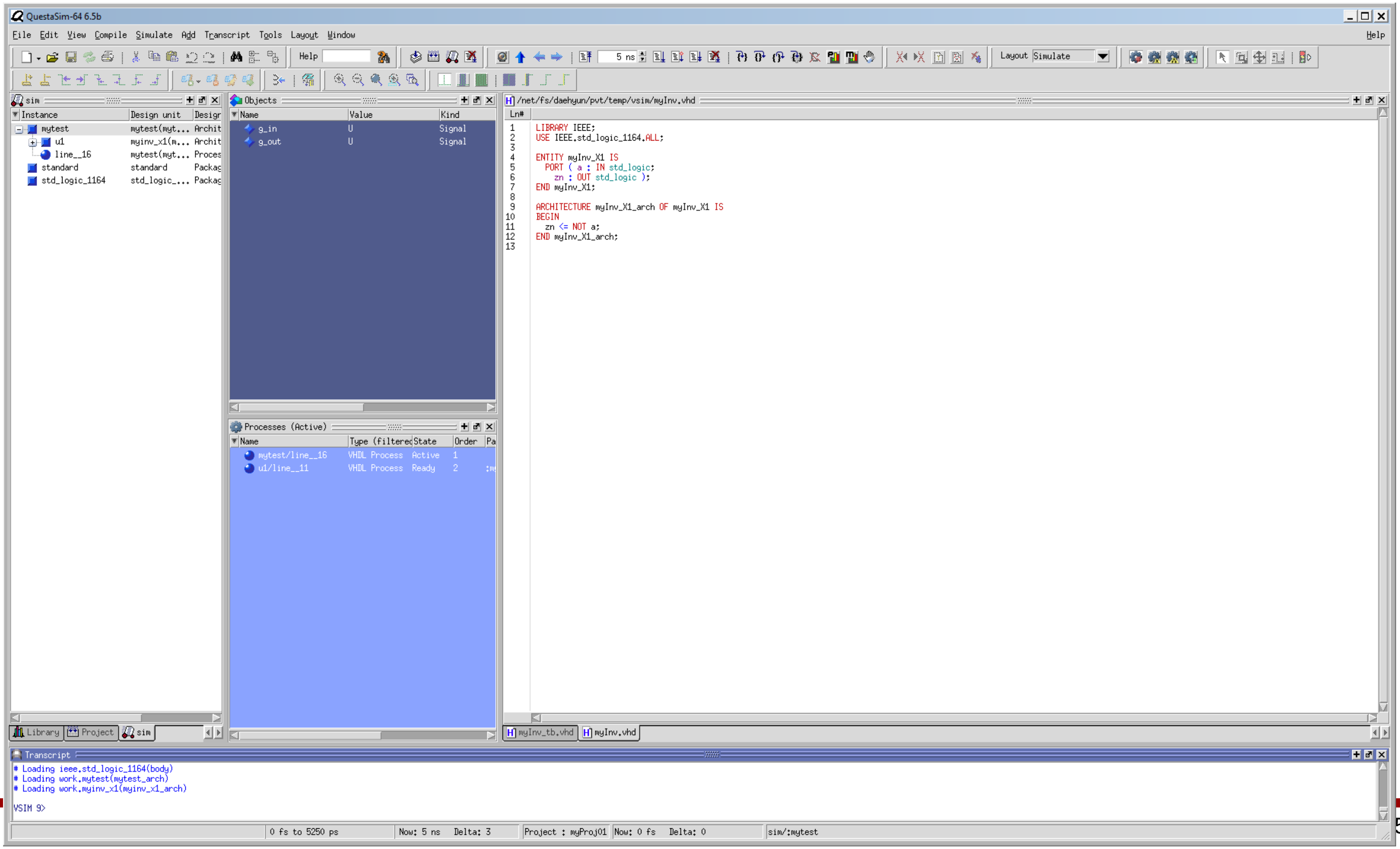


Name	Type	Path
work	Library	/net/
myinv_x1	Entity	/net/
mytest	Entity	/net/
mytest_arch	Architecture	
ARITHMETIC (unavailable)	Library	$AMS_
DISCIPLINES (unavailable)	Library	$AMS_
IEEE	Library	$AMS_

- Right-click “mytest_arch” and choose “Simulate”.

Simulation

- See the following window.



Instance	Design unit	Desigr
mytest	mytest(myt...	Archit
u1	myinv_x1(m...	Archit
line__16	mytest(myt...	Proces
standard	standard	Packag
std_logic_1164	std_logic_...	Packag

Name	Value	Kind
g_in	U	Signal
g_out	U	Signal

Name	Type (filtered	State	Order	Pa
mytest/line__16	VHDL Process	Active	1	
u1/line__11	VHDL Process	Ready	2	:m

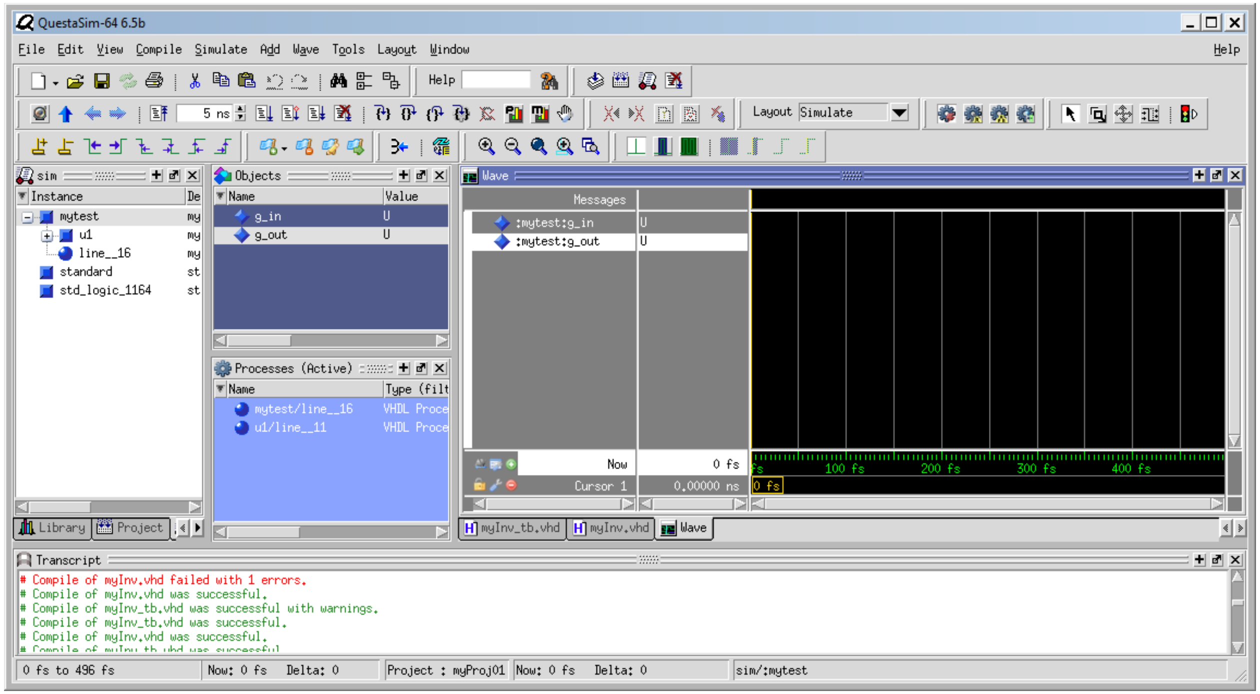
```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

ENTITY myInv_X1 IS
  PORT ( a : IN std_logic;
    zn : OUT std_logic );
END myInv_X1;

ARCHITECTURE myInv_X1_arch OF myInv_X1 IS
BEGIN
  zn <= NOT a;
END myInv_X1_arch;
```

```
# Loading ieee.std_logic_1164(body)
# Loading work.mytest(mytest_arch)
# Loading work.myinv_x1(myinv_x1_arch)

VSIM 9>
```

0 fs to 5250 ps | Now: 5 ns Delta: 3 | Project : myProj01 | Now: 0 fs Delta: 0 | sim/:mytest

Simulation

- Add a waveform window.
  - Click View → Wave.
- Then, drag and drop “g_in” and “g_out” to the waveform.

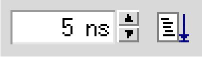


```
# Compile of myInv.vhd failed with 1 errors.
# Compile of myInv.vhd was successful.
# Compile of myInv_tb.vhd was successful with warnings.
# Compile of myInv_tb.vhd was successful.
# Compile of myInv.vhd was successful.
# Compile of myInv_tb.vhd was successful
```

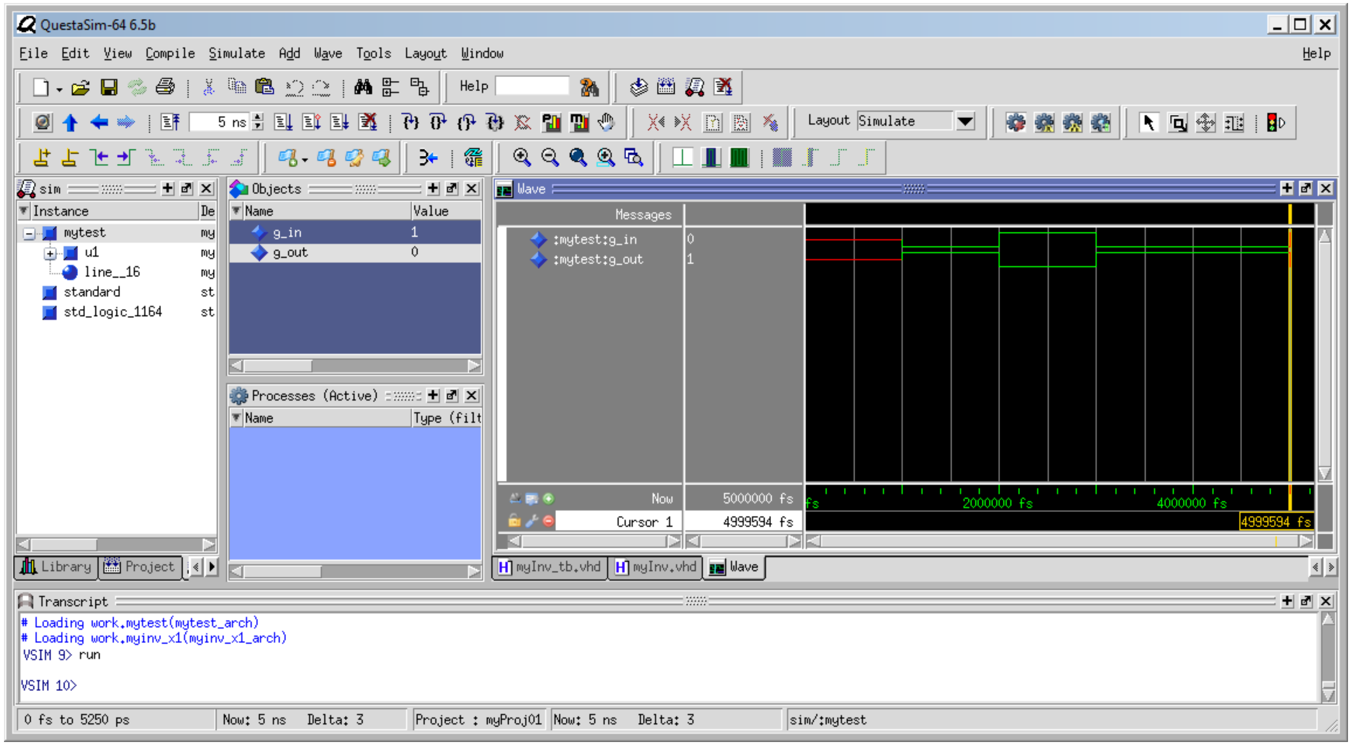
```
0 fs to 496 fs    Now: 0 fs    Delta: 0    Project : myProj01  Now: 0 fs    Delta: 0    sim/:mytest
```

Simulation

- Enter “5ns” in the Run Length window and click the Run icon.



- Click the waveform window and press “F” to zoom full.



Instance	De
mytest	my
u1	my
line__16	my
standard	st
std_logic_1164	st

Name	Value
g_in	1
g_out	0

Name	Type (filt

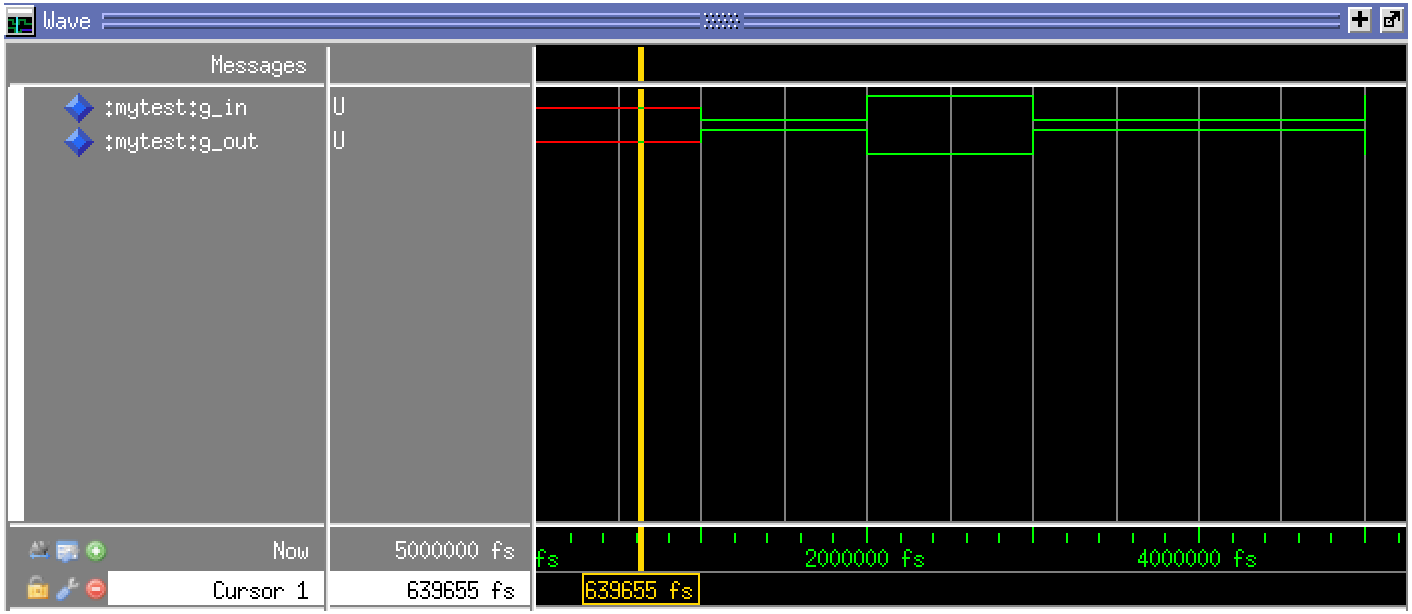
Messages	
:mytest:g_in	0
:mytest:g_out	1
Now	5000000 fs
Cursor 1	4999594 fs

```
# Loading work.mytest(mytest_arch)
# Loading work.myinv_x1(myinv_x1_arch)
VSIM 9> run

VSIM 10>
```

```
0 fs to 5250 ps    Now: 5 ns   Delta: 3    Project : myProj01  Now: 5 ns   Delta: 3    sim/:mytest
```

Simulation

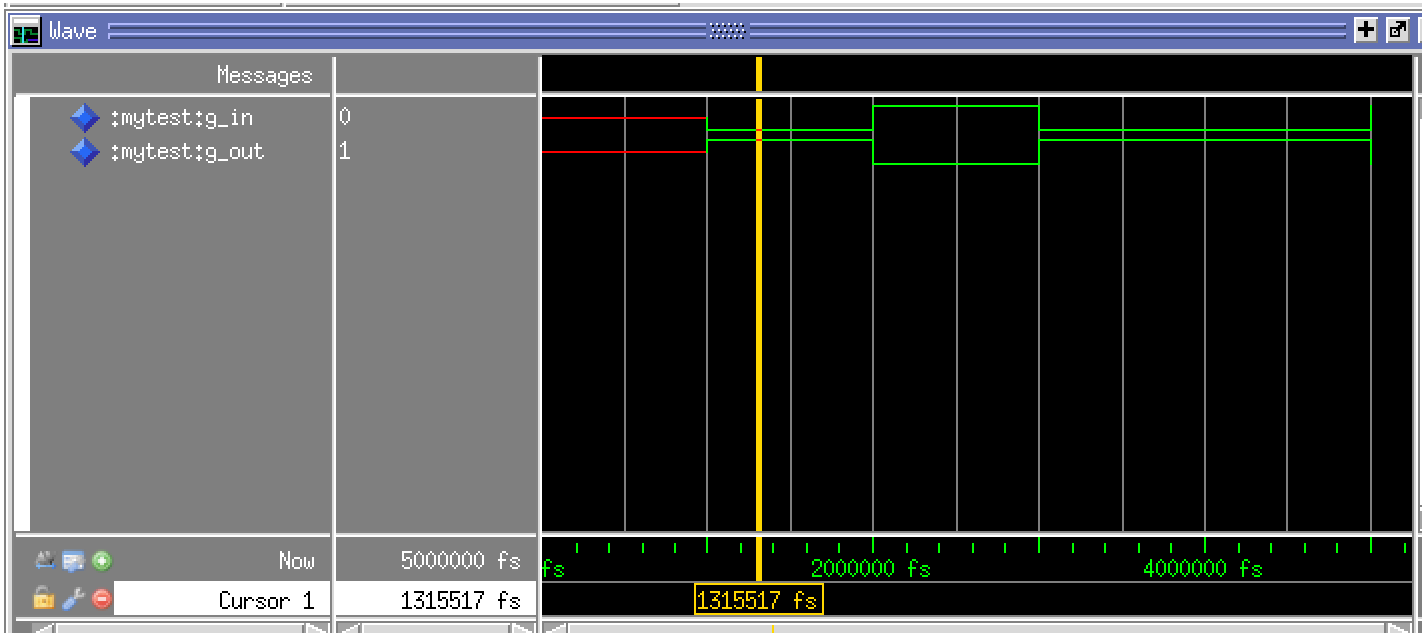
- Analysis
  - Initially, the input and output are unknown (U). Click somewhere between 0 and 1ns and check their values.



  - It is correct because we didn’t initialize the input.

Simulation

- At 1ns, we set g_in to 0, so we get 1 at the output.



```
Wave
Messages
:mytest:g_in    0
:mytest:g_out   1
Now        5000000 fs
Cursor 1   1315517 fs
```

Simulation

- Finish your simulation.
  - Simulate → End Simulation.