Homework Assignment 3

(Due Feb. 23rd at the beginning of the class)

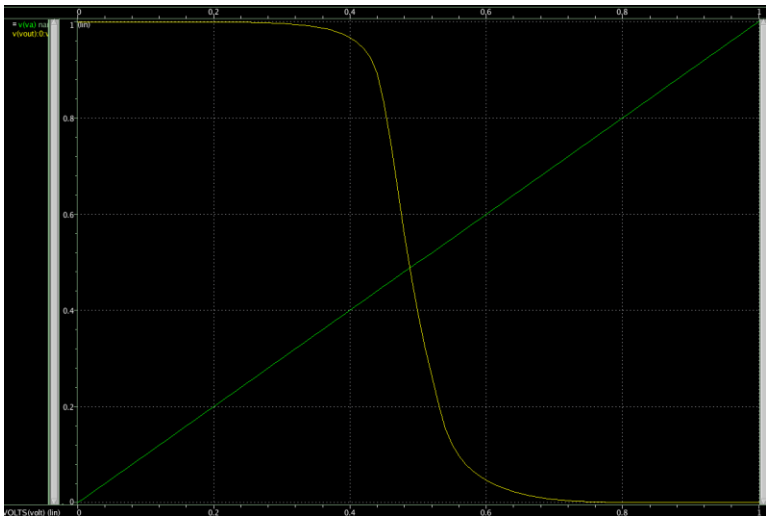
0. Preparation for homework 3
    - Download the following file into your working directory.
        - wget http://www.eecs.wsu.edu/~ee434/Homework/hw03.tar.gz
    - Unzip it.
        - tar xvzf hw03.tar.gz
    - Source synopsys.sh
        - source synopsys.sh

1. [Power Analysis, **10 points**]
    - Open inv_pwr.sp and see the netlist and the waveform of the source (Vsrc) and the two "measure" statements.
    - Run hspice to obtain average power consumed during the falling and rising transitions.
        - hspice inv_pwr.sp
    - It will generate some output files. See the waveform to make sure the output reaches 0 and V_{DD}.
        - wv inv_pwr.tr0
    - See the terminal. It prints out average power numbers as follows (for a 1X inverter and a 10fF load cap):

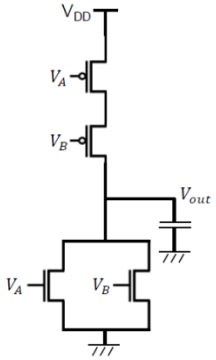
```
avg_power_fall=  5.1524E-06  from=  0.0000E+00     to=  1.0000E-09
avg_power_rise=  5.2038E-06  from=  1.0000E-09     to=  2.0000E-09
```

    - In my simulation, the average power for the falling transition is 5.15uW and that for the rising transition is 5.20uW.
    - [**Submit**] Average power for falling and rising transitions for 2X, 4X, 8X, and 16X inverters (load cap: 10fF).
    - [**Submit**] Average power for falling and rising transitions for 2X, 4X, 8X, and 16X inverters (load cap: 20fF).

2. [DC Analysis, **10 points**]
    - Open nand2_dc1_1.sp and see the netlist and the waveform of the sources (Vsrc1 and Vsrc2).
    - Run hspice and open the following file to see the DC characteristics of the 1X two-input NAND gate for V_A: $0 \rightarrow V_{DD}$ and V_B: V_{DD}.
        - wv nand2_dc1_1.sw0

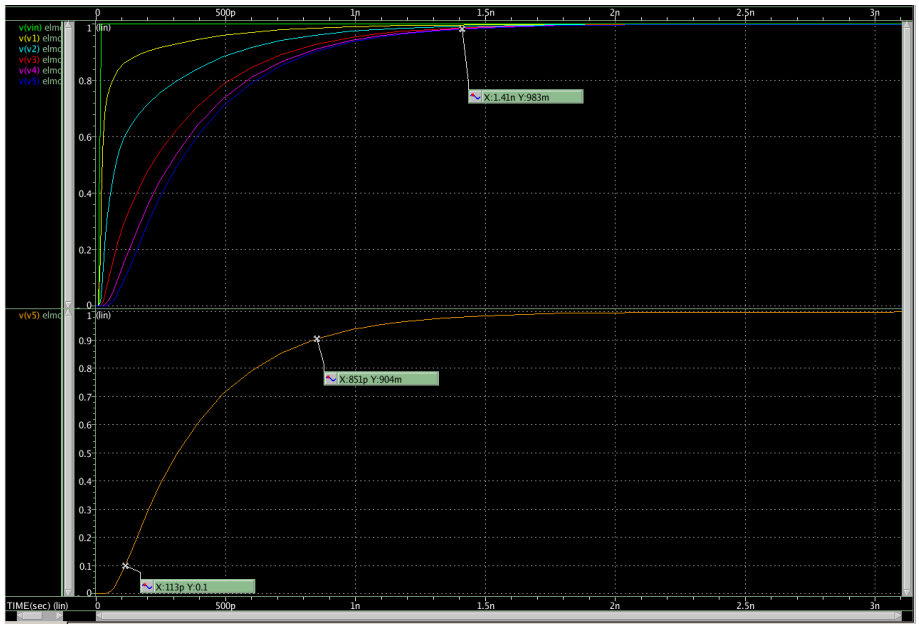


- Measure V_{IL}, V_{IH}, V_{OL}, and V_{OH}, and compute NM_L and NM_H. In my simulation, NM_L=345mV and NM_H=380mV.
- Open nand2_dc1_2.sp and see the netlist and the waveforms of the sources (Vsrc1 and Vsrc2). Run hspice and see the DC characteristics of the 1X two-input NAND gate for V_A: V_{DD} and V_B: 0→V_{DD}.
- Open nand2_dc2.sp and see the netlist and the waveform of the source (Vsrc1). Run hspice and see the DC characteristics of the 1X two-input NAND gate for V_A: 0→V_{DD} and V_B: 0→V_{DD}.
- [**Submit**] V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H for the following three cases for the 1x two-input NAND gate with a 10fF load cap:
    - Case 1) V_A: 0→V_{DD} and V_B: V_{DD}.
    - Case 2) V_A: V_{DD} and V_B: 0→V_{DD}.
    - Case 3) V_A: 0→V_{DD} and V_B: 0→V_{DD}.
- [**Submit**] Create a netlist for a 1X two-input NOR gate with a 10fF load cap. Obtain V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H for the following three cases:



    - Case 1) V_A: 0→V_{DD} and V_B: 0→V_{DD}.
    - Case 2) V_A: 0→V_{DD} and V_B: 0.
    - Case 3) V_A: 0 and V_B: 0→V_{DD}.

3. [Elmore Delay, **10 points**]
    - Open elmore_ex.sp and see the netlist.
    - Run hspice and open the waveform to measure 10%-90% rise time.
        - hspice elmore_ex.sp
        - wv elmore_ex.tr0
    - The following shows the waveforms I obtained at each node.



    - The 10%-90% rise time in my simulation is approximately 724ps.
    - The RC time constant for the given RC tree is 397ps. Then, 10%-90% rise time computed by the Elmore delay model is 2.2*397ps = 873.4ps, so the error is 873ps – 724ps = +149ps (overestimation).
    - [**Submit**] 10%-90% rise time of the RC tree in elmore_s.sp (at Vout) obtained by hspice simulation. 10%-90% rise time of the RC tree approximated by the Elmore delay model.
    - [**Submit**] 10%-90% rise time of the RC tree in elmore_m.sp (at Vout1 and Vout2) obtained by hspice simulation. 10%-90% rise time of the RC tree approximated by the Elmore delay model.
    - [**Submit**] In all the above simulations, we use 10ps for the rising transition time at the input. Now, open elmore_ex.sp and change the input rising transition time from 10ps to 100ps. Run hspice again and obtain 10%-90% rise time at Vout. Compare this with the rise time I obtained above (724ps). Is the delay dependent on the input transition time? Obtain 10%-90% rise time for the following input transition times (200ps, 300ps, 400ps, 500ps).

4. [Transient Analysis of Transmission Gates, **10 points**]
    - In this problem, we will simulate transmission gates.

- Open tr_1.sp and see the netlist.
- Simulate tr_1.sp and obtain rise/fall times. In my simulation, I got 264ps (fall) and 290ps (rise).
- [**Submit**] Upsize the transmission gate to 2X and obtain rise/fall times.
- [**Submit**] Upsize the transmission gate to 4X and obtain rise/fall times.

5. [Analysis of Pass Transistors, **10 points**]
    - Open pt_1.sp and see the netlist. There is one pass transistor.
    - [**Submit**] Simulate pt_1.sp and obtain 10%-60% rise time. If you use the "measurement tool" in WaveView and set H(%) to 60.00, it will measure 10%-55% rise time, but this is acceptable. Submit the 10%-60% rise time.
    - [**Submit**] Obtain 10%-60% rise time for the following pass transistor sizes: 2X, 4X, 8X.
    - [**Submit**] Add one more pass transistor between the existing pass transistor and the output capacitor. Set the sizes of the two pass transistors (the existing one and the new one) to 1X. Obtain 10%-60% rise time. Upsize them to 2X, 4X, and 8X, and obtain 10%-60% rise time.
    - [**Submit**] Add two more pass transistors between the new pass transistor you added above and the output capacitor (so there are total four pass transistors between the output of the inverter and the output capacitor). Obtain 10%-60% rise time for 1X, 2X, 4X, and 8X pass transistor sizes.