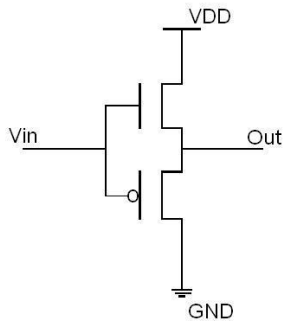
EE 434
Homework Assignment 1
(Due Friday, 6th September 2013 at the beginning of the class)

(1) Given the choice between NOR and NAND logic, which one would you prefer for implementation in static CMOS? Which one would you prefer in pseudo-NMOS? Explain. **(5 points)**

(2) Implement a two-input MUX using static CMOS and Transmission gate logic. Which one needs more transistors? **(5 points)**

(3) What is the intended function of the circuit shown in the figure below? What is the output swing? **(5 points)**

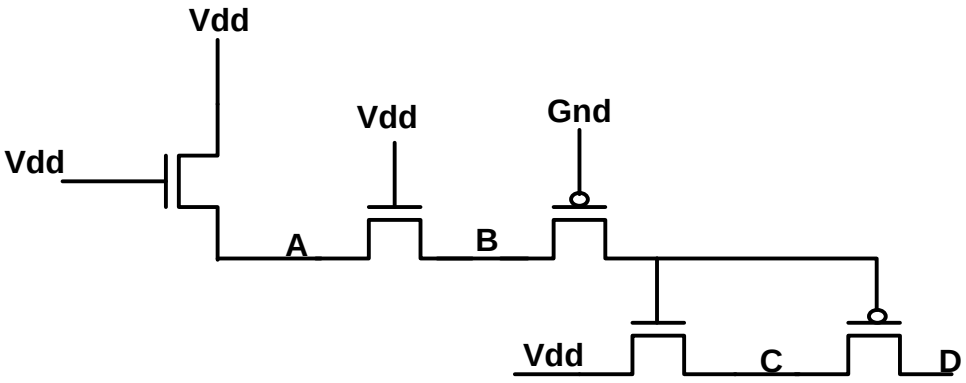


(4) Design a pseudo-NMOS gate that implements the following function

$F = \overline{A(B+C+D)+E \bullet F \bullet G}$ **(5 points)**

(5) A static CMOS NOR gate uses 4 transistors, while a pseudo-NMOS gate uses only 3. But as discussed in class, pseudo-NMOS has its own problems. Design a NOR gate using 3 transistors that does not have the problems of the pseudo-NMOS. You can assume that both the inputs and their complements are available. **(5 points)**

(6) Determine the voltage levels at the nodes A, B, C and D in the following circuit. **(4 points)**



(7) Multiple-output Domino Logic: Implement the following three functions

(C + D)

B (C + D)

AB (C + D)

using a single domino logic. **(6 points)**

(8) Size the transistors (in terms of W) in a three-input static CMOS NOR gate such that the circuit's rise and fall times are approximately equal.

(5 points)