EE434

ASIC and Digital Systems

Midterm Exam 1

February 25, 2015. (5:10pm – 6pm)

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Name:

WSU ID:

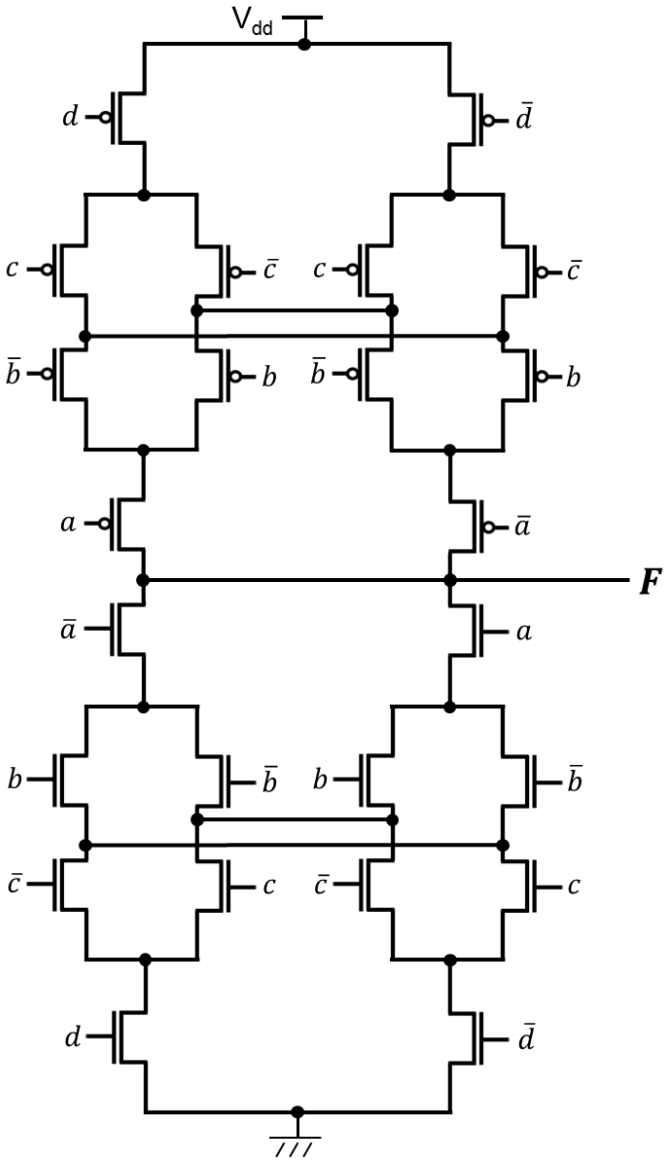
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
Total	80	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

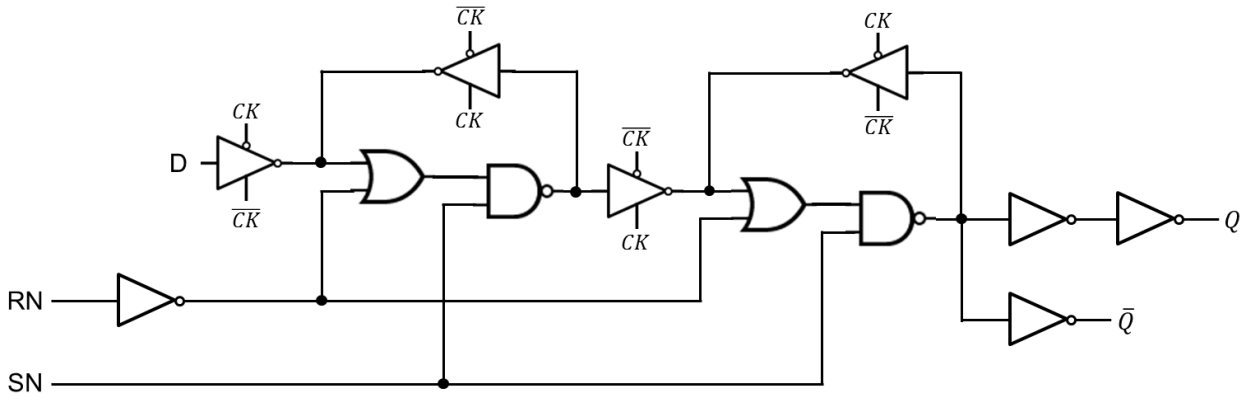
Problem #1 (Static CMOS gates, 10 points).

Represent F as a function of $a, b, c,$ and d.



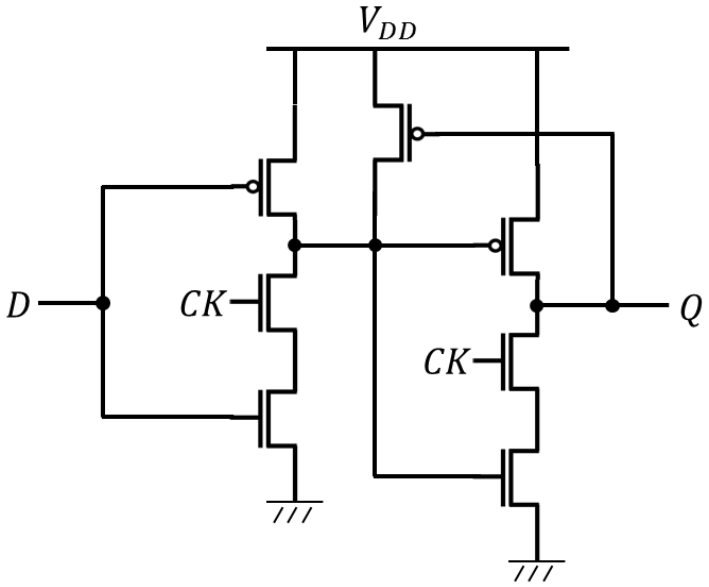
Problem #2 (Static CMOS gates, 10 points).

What does the following circuit do? Describe the function of the circuit in as much detail as possible.



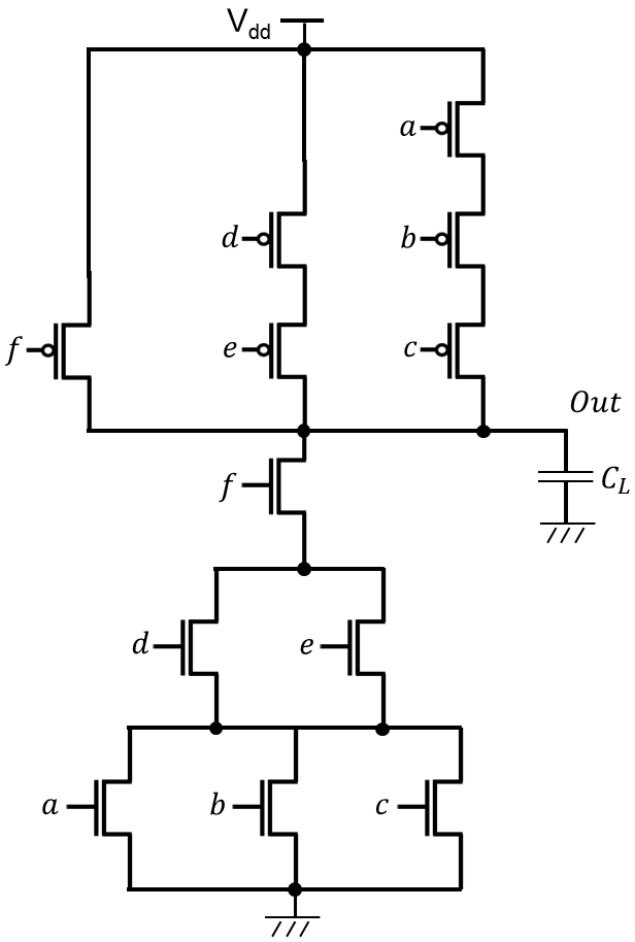
Problem #3 (CMOS Logic, 10 points).

What is the functionality of the following circuit? Describe the functionality in as much detail as possible.



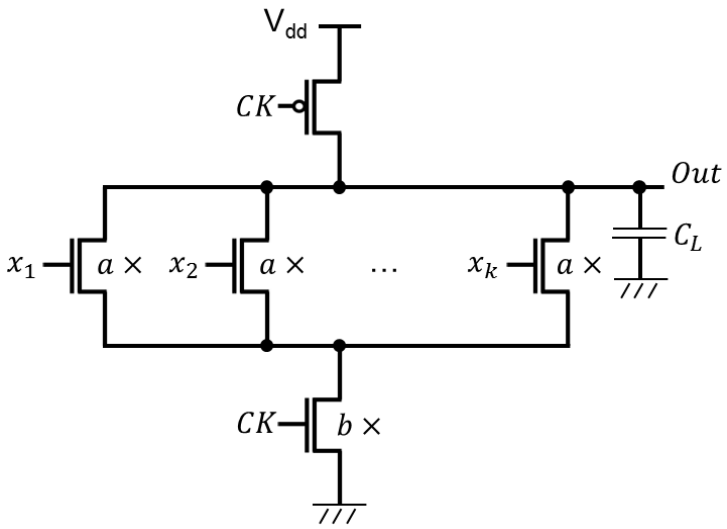
Problem #4 (Transistor Sizing, 10 points).

Size the transistors in the following gate. R_n is the resistance of a 1X NMOS transistor. $\mu_n = 2 \cdot \mu_p$. Ignore all the parasitic capacitances. Target time constant: $\tau_{target} = R_n \cdot C_L$. Try to minimize the total area.



Problem #5 (Transistor Sizing, 10 points).

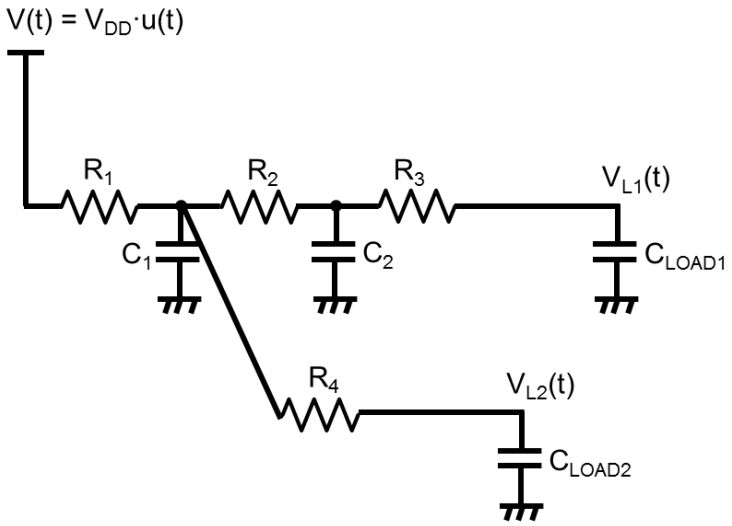
We want to design a *k*-input NOR gate. However, the static CMOS gate design methodology is not suitable for the design of the *k*-input NOR gate due to area overhead in the pull-up network and the body-bias effect. Therefore, we are going to design it using the dynamic CMOS design methodology. The following shows a schematic of the *k*-input NOR gate.



R_n is the resistance of a 1X NMOS transistor. $\mu_n = 2 \cdot \mu_p$. Ignore all the parasitic capacitances. Target time constant: $\tau_{target} = R_n \cdot C_L$. All the transistors for x_1 ~ x_k are upsized to aX and the transistor for CK is upsized to bX (a and b are ***real*** numbers). We *minimize* the total width, $Width = a \cdot k + b$. Find a and b (i.e., derive a (and b) as a function of k) minimizing the total width.

Problem #6 (Elmore Delay, 10 points).

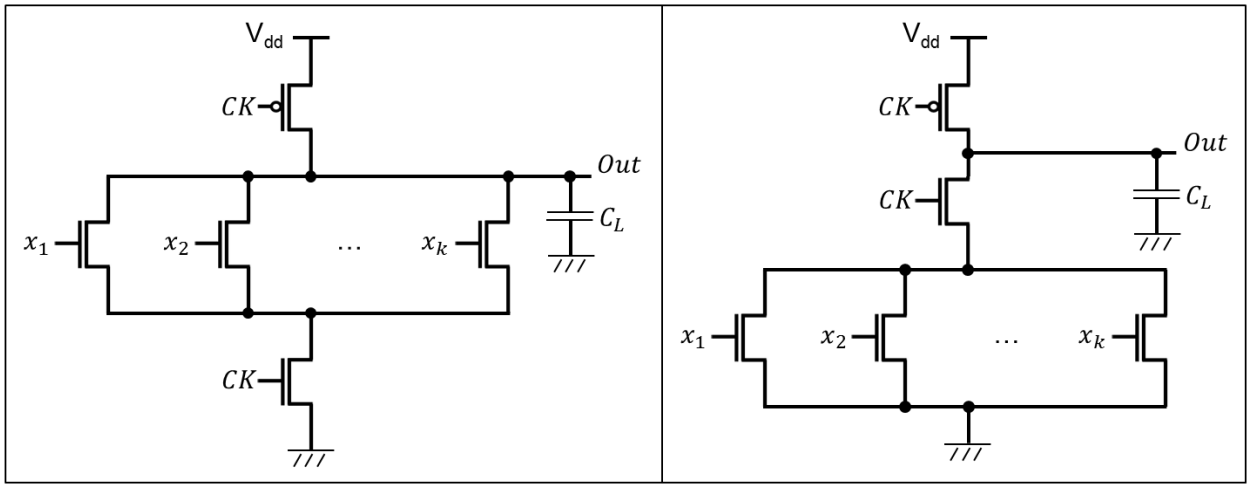
6-1. Compute Elmore delay at LOAD1 and LOAD2, i.e., represent the delay at LOAD1 (and LOAD2) as a function of $R_1 \sim R_4, C_1, C_2, C_{LOAD1}$, and C_{LOAD2}.



6-2. Compute Elmore delay at LOAD1 for $R_1 = R_2 = R_3 = 1k\Omega, C_1 = C_2 = C_{LOAD1} = 10fF, R_4 = \mathbf{0.1k\Omega}, and\ C_{LOAD2} = 1pF$. Then, compute Elmore delay at LOAD1 for $R_1 = R_2 = R_3 = 1k\Omega, C_1 = C_2 = C_{LOAD1} = 10fF, R_4 = \mathbf{10M\Omega}, and\ C_{LOAD2} = 1pF$. This result is called “resistive shielding”. Discuss a limitation of the Elmore delay model in terms of the resistive shielding effect.

Problem #7 (Dynamic CMOS, 10 points).

Compare the following implementations for a dynamic-CMOS *k*-input NOR gate. Are there any problems in (a)? in (b)?



(a) (b)

Problem #8 (DC Characteristics, 10 points).

The following circuit is called “pseudo-PMOS”. Sketch a DC characteristic curve of the pseudo-PMOS inverter and properly split the curve into regions. In each region, show the status (cut-off, linear, saturation) of each transistor (m_n and m_p).