EE434

ASIC and Digital Systems

Midterm Exam 1

March 7, 2015. (5:10pm – 6pm)

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Name:

WSU ID:

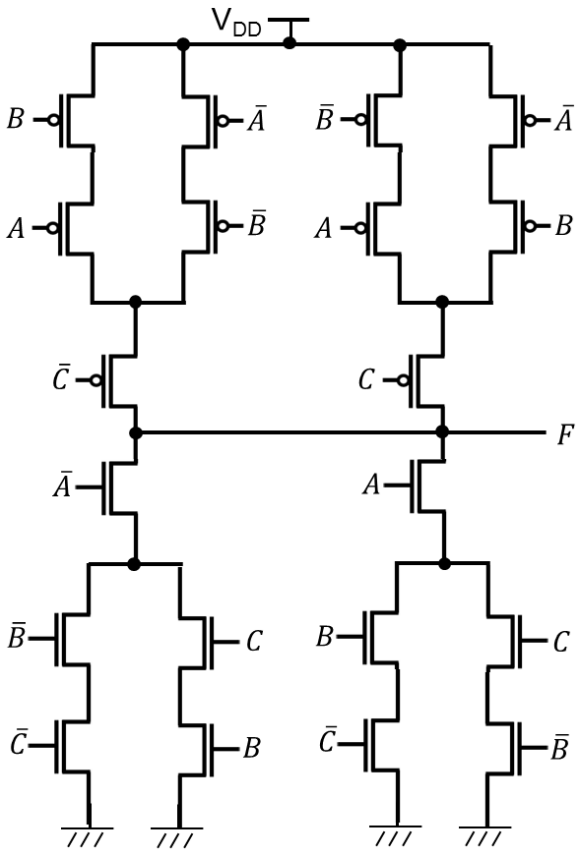
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
Total	80	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

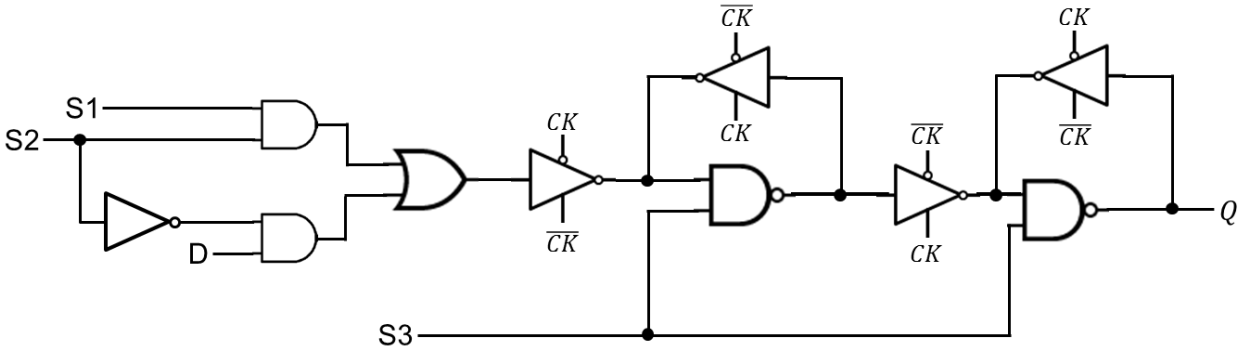
Problem #1 (Static CMOS gates, 10 points).

Represent F as a Boolean function of A, B, and C.



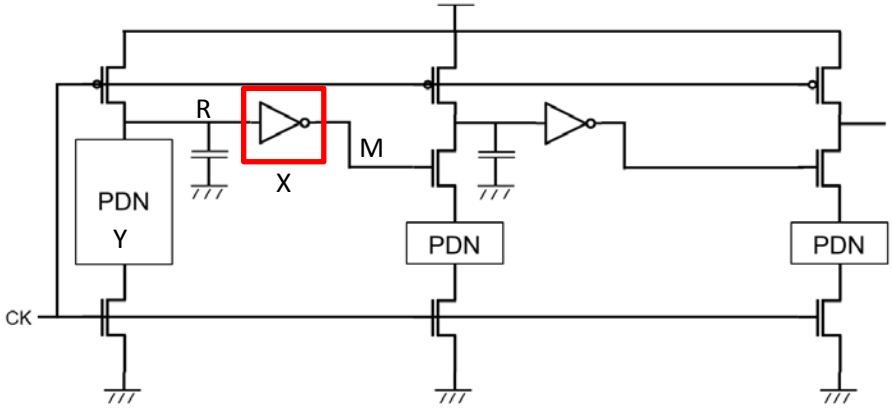
Problem #2 (Static CMOS gates, 10 points).

What does the following circuit do? Describe the function of the circuit in as much detail as possible (CK is a clock signal).



Problem #3 (Domino Logic and DC Characteristics, 10 points).

The following shows a general three-stage domino logic. When CK is 0, the logic precharges all internal nodes, so node R is 1 and node M is 0. In general, the PMOS transistors for precharging are properly upsized. When CK is 1, the logic evaluates the PDNs. When the PDN Y is true, it discharges node R, so R becomes 0 and M becomes 1. However, the PDNs in the logic are cascaded, so the PDNs should switch quite fast. Thus, the NMOS transistors in the PDNs are also properly upsized.

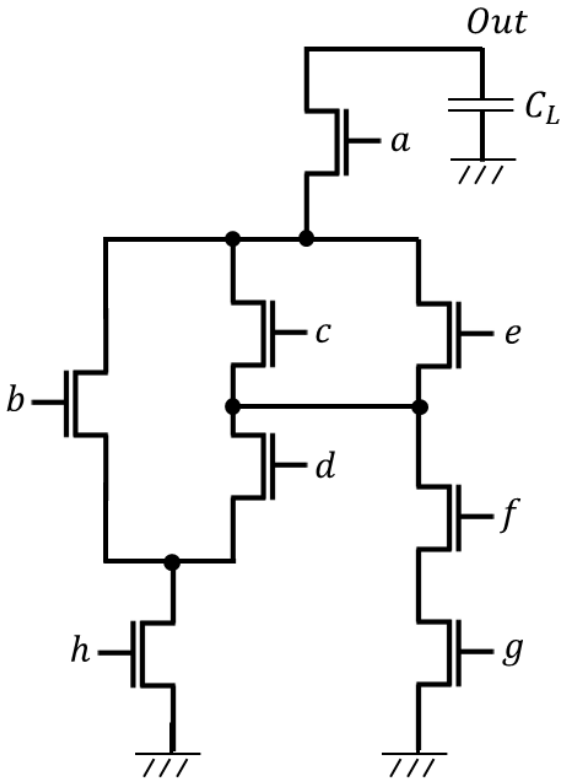


The NMOS transistor of inverter X can be small because it is used to discharge node M, which has a sufficiently small capacitance, during precharging. However, the PMOS transistor of inverter X should be properly upsized (e.g., by 16X) because it is used to charge node M during evaluation, so its switching time should be very short.

Question) Does this size imbalance (e.g., NMOS: 1X, PMOS: 16x) of inverter X cause any DC characteristics (noise margin) problems for inverter X? Explain why it causes (or does not cause any) DC characteristics (noise margin) problems for inverter X.

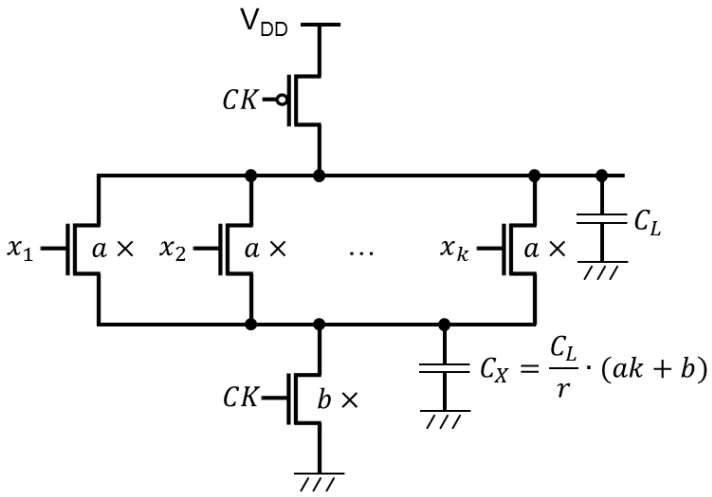
Problem #4 (Transistor Sizing, 10 points).

Size the transistors in the following pull-down network. R_n is the resistance of a 1X NMOS transistor. Ignore parasitic capacitances. Target time constant: $\tau_{target} = R_n \cdot C_L$. Try to minimize the total area.



Problem #5 (Transistor Sizing, 10 points).

We want to design a *k*-input NOR gate. However, the static CMOS gate design methodology is not suitable for the design of the *k*-input NOR gate. Thus, we are going to design it using the dynamic CMOS design methodology. The following shows a schematic of the *k*-input NOR gate.



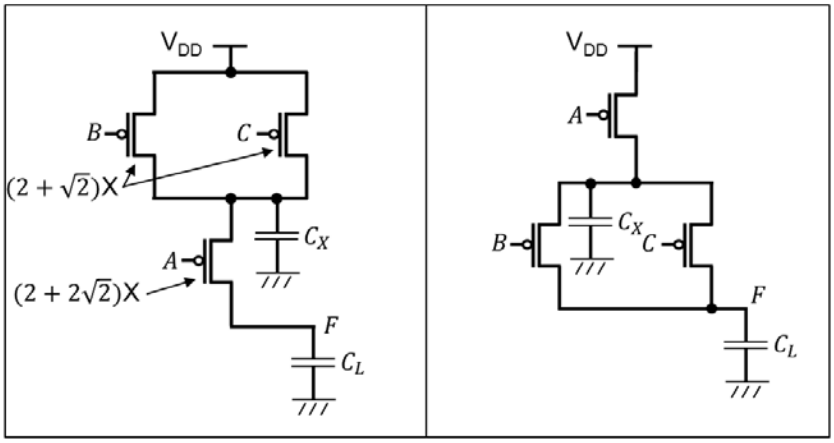
R_n is the resistance of a 1X NMOS transistor. Target time constant: $\tau_{target} = R_n \cdot C_L$. All the transistors for $x_1 \sim x_k$ are upsized to aX and the NMOS transistor for CK is upsized to bX (a and b are ***real*** numbers). Unfortunately, the parasitic capacitance at the internal node shown above is proportional to the sum of the width of the transistors connected to the node. Thus, the parasitic capacitance C_X at the internal node is $C_X = \frac{C_L}{r} \cdot (ak + b)$ where C_L is the load cap and r is a constant ($r > 1$). We ***minimize*** the total width

$$Width = a \cdot k + b.$$

Find a minimizing the total width (i.e., represent a as a function of k and r).

Problem #6 (Switching Characteristics, 10 points).

We design $F = \overline{A + B \cdot C}$ using the static CMOS gate design style. The following shows a transistor-level schematic of the pull-up network of the design:

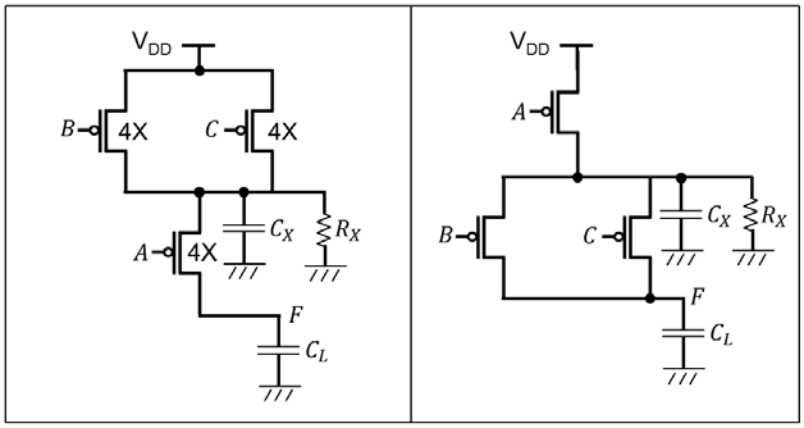


Both (a) and (b) are functionally equal. The internal node in the pull-up network has parasitic capacitance C_X. Since the parasitic capacitance of an internal node is generally determined by the size of the transistors connected to the node, both (a) and (b) have the same parasitic capacitance C_X. R_n is the resistance of a 1X NMOS transistor. $\mu_n = 2\mu_p$. Target time constant: $\tau_{target} = R_n \cdot C_L$. If we optimally size the pull-up network to minimize the total width without considering C_X, the pMOS A is upsized to $\left(2 + 2\sqrt{2}\right)$X and the pMOS B and C are upsized to $(2 + \sqrt{2})$X as shown in the figure.

Compute the worst-case rise time in (a) and in (b) considering C_x, i.e., represent the worst-case rise time as a function of R_n, C_L, and C_x. Which design has shorter rise time?

Problem #7 (Power Consumption, 10 points).

We design $F = \overline{A + B \cdot C}$ using the static CMOS gate design style. The following shows a transistor-level schematic of the pull-up network of the design:



Both (a) and (b) are functionally equal. The internal node in the pull-up network has parasitic capacitance C_X and also a parasitic resistance R_X connected to the ground (this is a leaky path, i.e., even if A=B=C=1 and $C_X = V_{\mathrm{DD}}$, C_X will be slowly discharged through R_X). All the transistors are upsized by 4X as shown in the figure. The following table shows the probability that each input signal is 0 or 1:

	0	1
A	0.8	0.2
B	0.2	0.8
C	0.2	0.8

We want to minimize power consumption (both dynamic and leakage power) of the gate. Which design do you prefer? (a) or (b)? Select one of them and explain why you prefer the design to minimize power consumption. You can qualitatively and intuitively explain it (without performing accurate probability computation).

Problem #8 (Pass-Transistor Logic, 10 points).

Represent F as a Boolean function of A, B, and C.