EE434

ASIC and Digital Systems

Midterm Exam 2

April 8, 2016. (5:10pm – 6pm)

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Name:

WSU ID:

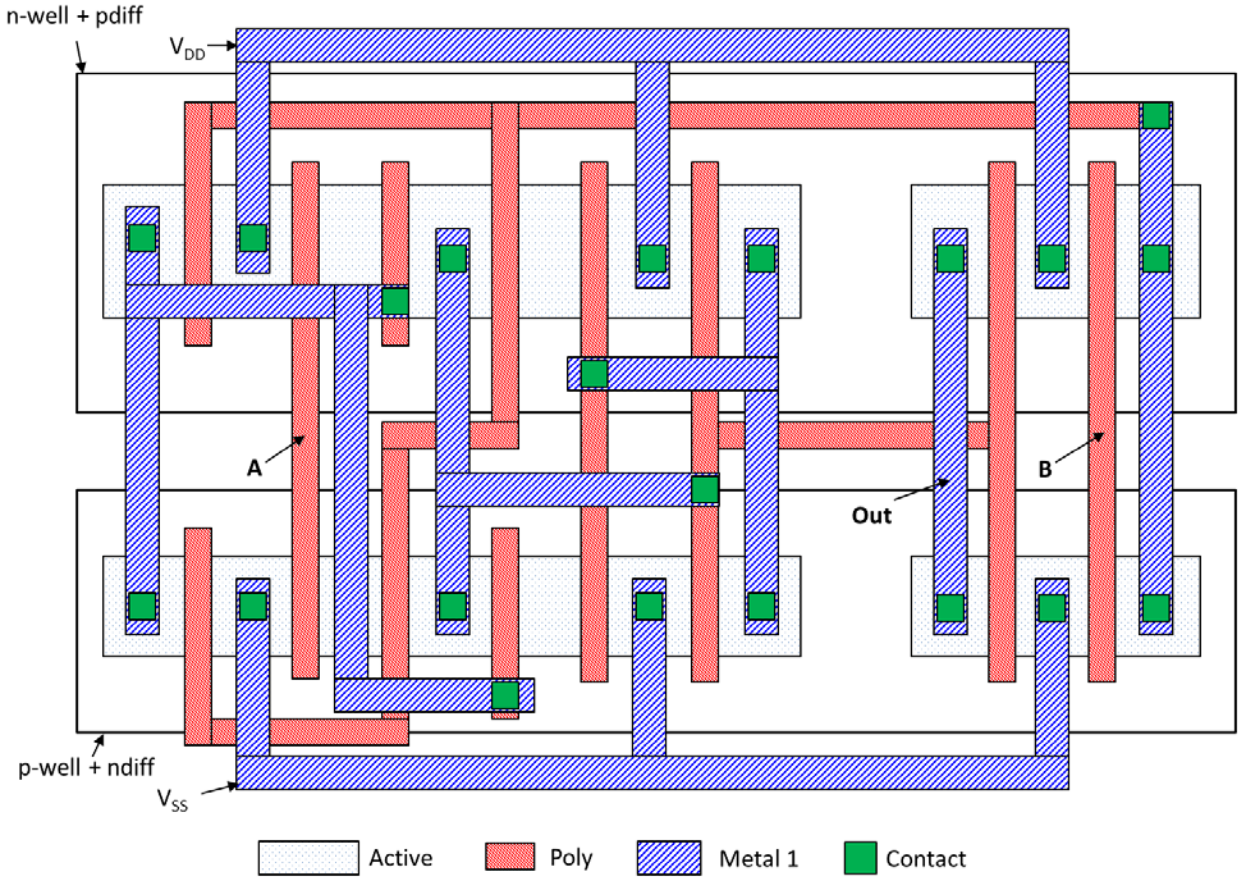
Problem	Points	
1	15	
2	15	
3	15	
4	10	
5	13	
6	12	
Total	80	

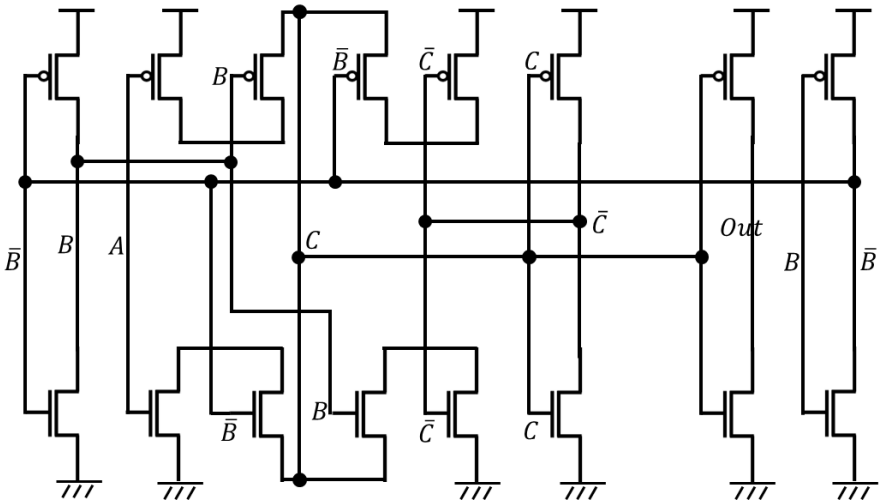
* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

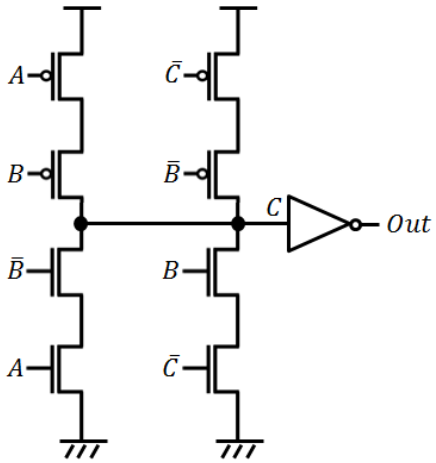
Problem #1 (Layout, 15 points).

Represent Out as a Boolean function of A and B or describe the function of the following layout in as much detail as possible (Primary inputs: A, B. Primary output: Out).





After further simplification, we get the following:



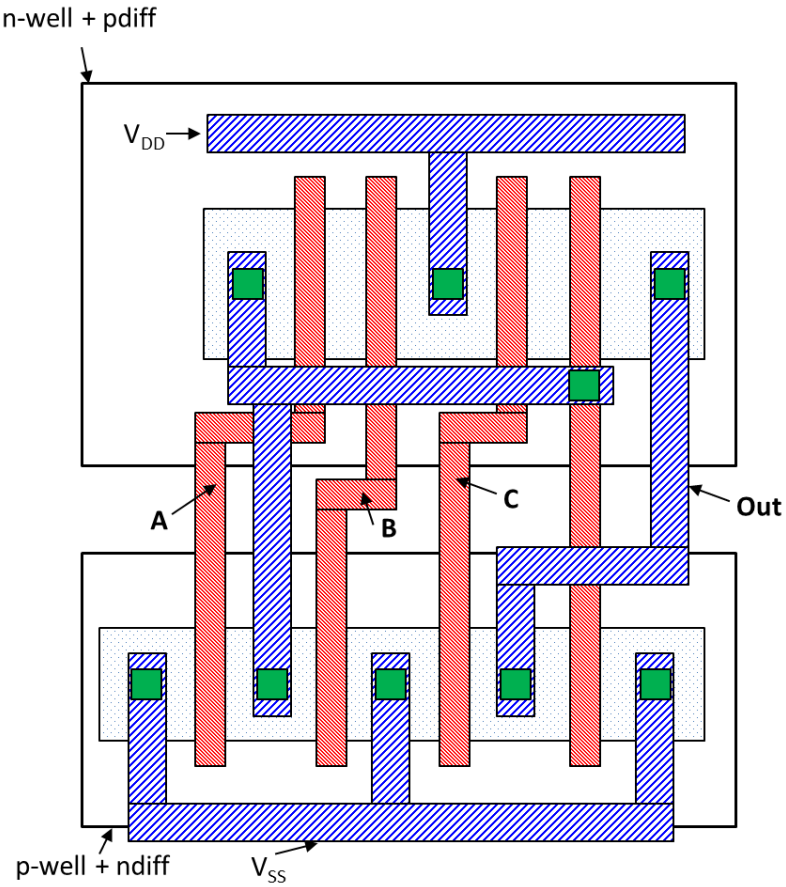
If B=1, the output holds the current value.

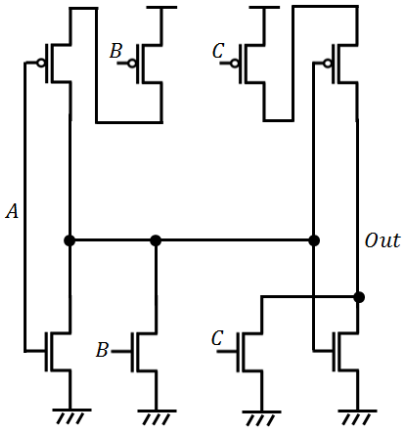
If B=0, the output is $\bar{C}$, which is A, so the output follows A.

=> Thus, this is an active-low D-latch (A is a signal input and B is an enable or CK signal).

Problem #2 (Layout, 15 points).

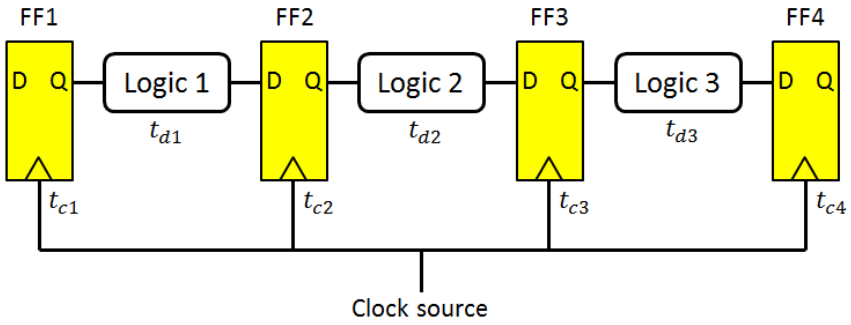
Represent Out as a Boolean function of A, B and C or describe the function of the following layout in as much detail as possible (Primary inputs: A, B, C. Primary output: Out).





$Out = \overline{(\overline{A + B}) + C} = (A + B) \cdot \bar{C}$

Problem #3 (Timing Analysis, 15 points).



Four flip-flops are connected as shown above.

- Clock period: $t_{CLK} = 500ps$
- F/F internal delay: $t_{CQ} = 50ps$
- Setup time of each F/F: $t_s = 50ps$
- Delay of Logic 1: $t_{d1} = 450ps$
- Delay of Logic 2: $t_{d2} = 480ps$
- Delay of Logic 3: $t_{d3} = 250ps$
- Delay of the clock from the clock source to FF1: $t_{c1} = 400ps$
- Delay of the clock from the clock source to FF#: $t_{c\#}$ (#=2, 3, 4)

Since the delays of Logic 1 and Logic 2 are too large, Logic 1 and Logic 2 will violate the setup time constraint if the clock skew is zero (i.e., $t_{c1} = t_{c2} = t_{c3} = t_{c4}$). To resolve this issue, we want to intentionally use the clock skew. However, we also want to minimize the total clock delay ($t_{c1} + t_{c2} + t_{c3} + t_{c4}$) to minimize the clock power consumption. Find t_{c2}, t_{c3}, and t_{c4} that satisfies the setup time constraint and minimizes the total clock delay ($t_{c1} + t_{c2} + t_{c3} + t_{c4}$).

1) To satisfy the setup time constraint of FF2, the following inequality should hold:

$$t_{CQ} + t_{d1} \le t_{CLK} - t_s + (t_{c2} - t_{c1}) \quad \Rightarrow \quad 450ps \le t_{c2} \quad \Rightarrow \quad t_{c2} = 450ps + \delta_2 \quad (\delta_2 > 0)$$

2) To satisfy the setup time constraint of FF3, the following inequality should hold:

$$t_{CQ} + t_{d2} \le t_{CLK} - t_s + (t_{c3} - t_{c2}) \quad \Rightarrow \quad t_{c2} + 80ps \le t_{c3} \quad \Rightarrow$$

$$t_{c3} = (450ps + \delta_2) + 80ps + \delta_3 = 530ps + \delta_2 + \delta_3 \quad (\delta_3 > 0)$$

3) To satisfy the setup time constraint of FF4, the following inequality should hold:

$$t_{CQ} + t_{d3} \le t_{CLK} - t_s + (t_{c4} - t_{c3}) \quad \Rightarrow \quad t_{c3} - 150ps \le t_{c4} \quad \Rightarrow$$

$$t_{c4} = (530ps + \delta_2 + \delta_3) - 150ps + \delta_4 = 380ps + \delta_2 + \delta_3 + \delta_4 \quad (\delta_4 > 0)$$

The total clock delay = $t_{c1} + t_{c2} + t_{c3} + t_{c4} = (400ps) + (450ps + \delta_2) + (530ps + \delta_2 + \delta_3) + (380ps + \delta_2 + \delta_3 + \delta_4)$

To minimize the total clock delay, we set δ_2, δ_3, and δ_4 to zero. Then, we obtain

$$t_{c2} = 450ps, \qquad t_{c3} = 530ps, \qquad t_{c4} = 380ps$$

Problem #4 (Timing Analysis, 10 points).

Can a path have both setup and hold time violations at the same time? Yes/No. Explain why.

A setup time constraint for a path is as follows:

$$t_{LOGIC} \leq t_{CLK} - t_s - t_{CQ} + t_{skew}$$

A hold time constraint for the same path is as follows:

$$t_{LOGIC} \geq t_h - t_{CQ} + t_{skew}$$

Combining both results in:

$$t_h - t_{CQ} + t_{skew} \leq t_{LOGIC} \leq t_{CLK} - t_s - t_{CQ} + t_{skew}$$

Thus, violating both means:

$$1)\ t_{LOGIC} < t_h - t_{CQ} + t_{skew}$$

$$2)\ t_{LOGIC} > t_{CLK} - t_s - t_{CQ} + t_{skew}$$

which leads to:

$$t_{CLK} - t_s - t_{CQ} + t_{skew} < t_h - t_{CQ} + t_{skew}$$

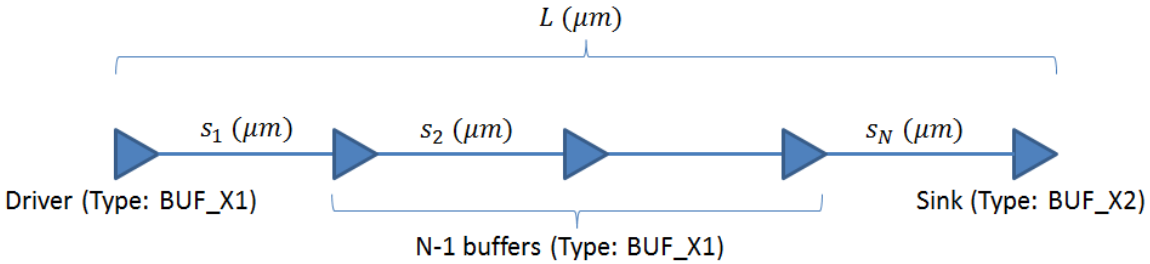
$$\Rightarrow\ t_{CLK} - t_s < t_h$$

$$\Rightarrow\ t_{CLK} < t_h + t_s$$

Thus, it is THEORETICALLY possible if the clock period is less than the sum of the hold and setup times.

(Of course, this won't happen in reality because the clock period is much greater than $t_h + t_s$).

Problem #5 (Interconnect, 13 points).



A source (type: BUF_X1) drives a sink (type: BUF_X2) through a net and you are supposed to ***optimally*** insert N-1 buffers (type: BUF_X1) between them. Find the number of buffers to insert (i.e., find N) and the optimal locations of the buffers (i.e., find $s_1, s_2, \ldots, s_N$) minimizing the total delay.

- Output resistance of BUF_X1: R_1
- Input capacitance of BUF_X1: C_1
- Input capacitance of BUF_X2: C_2
- Total length of the net: L (um)
- Unit wire resistance: r_w
- Unit wire capacitance: c_w

Suppose s_N is known. Then, the N-2 buffers between the driver and the (N-1)-th buffer should be evenly distributed to minimized the delay. Thus, we simply get

$$s_1 = s_2 = \cdots = s_{N-1} = k$$

The sum of the delays of the first (N-1) segments is

$$\tau_L = (N-1)\{R_1(k \cdot c_w + C_1) + k \cdot r_w \cdot C_1 + 0.5 \cdot r_w \cdot c_w \cdot k^2\}$$

and the delay of the rightmost segment is

$$\tau_R = R_1((L-(N-1)k) \cdot c_w + C_2) + (L-(N-1)k) \cdot r_w \cdot C_2 + 0.5 \cdot r_w \cdot c_w \cdot \{L-(N-1)k)^2\}$$

so the total delay is

$$\tau = R_1\{c_w L + C_1(N-1) + C_2\} + r_w\{C_2 L + k(N-1)(C_1 - C_2)\} + 0.5 \cdot r_w \cdot c_w\{(N-1)k^2 + (L-(N-1)k)^2\}$$

and

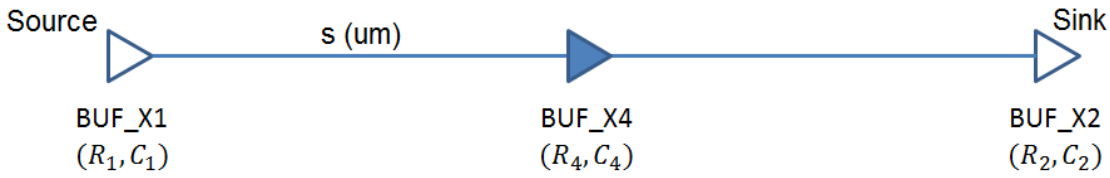
$$\frac{d\tau}{dk} = 0 = r_w(C_1 - C_2)(N-1) + r_w \cdot c_w \cdot \{k(N-1) - (N-1)L + k(N-1)^2\}$$

$$\Rightarrow \quad k = \frac{(C_2 - C_1) + c_w L}{c_w \cdot N}$$

Thus, $s_1 = s_2 = \cdots = s_{N-1} = \frac{(C_2 - C_1) + c_w L}{c_w \cdot N}$, $\quad s_N = L - k \cdot (N-1) = \frac{c_w \cdot L - (N-1) \cdot (C_2 - C_1)}{c_w \cdot N}$

Problem #6 (Interconnect, 12 points).

A source (type: BUF_X1) drives a sink (type: BUF_X2) through a net and we want to *optimally* insert a buffer (type: BUF_X4) between them to minimize the total signal delay as shown in the figure below. s is the distance between the source and the buffer. Answer the following questions.



- Output resistance of each cell: $R_{\#}$ ($R_1 > R_2 > R_4$)
- Input capacitance of each cell: $C_{\#}$ ($C_1 < C_2 < C_4$)
- Unit wire resistance and capacitance: r_w, c_w

1) If R_4 goes up, s should go up. (**True**/False)

If R_4 goes up, the delay of the right segment goes up. To reduce it, we should move BUF_X4 to the right.

2) If C_4 goes up, s should go up. (True/**False**)

If C_4 goes up, the delay of the left segment goes up. To reduce it, we should move BUF_X4 to the left.

3) If R_1 goes up, s should go up. (True/**False**)

If R_1 goes up, the delay of the left segment goes up. To reduce it, we should move BUF_X4 to the left.

4) If C_2 goes up, s should go up. (**True**/False)

If C_2 goes up, the delay of the right segment goes up. To reduce it, we should move BUF_X4 to the right.

5) If r_w goes up, s should go up. (**True**/False)

If r_w goes up, the impact of R_1 and R_4 goes down. Thus, it is better to move the buffer to the center point, so should move BUF_X4 to the right.

6) If c_w goes up, s should go up. (**True**/False)

If c_w goes up, the impact of C_4 and C_2 goes down. Thus, it is better to move the buffer to the center point, so we should move BUF_X4 to the right.

We can analyze it quantitatively too. The delay of the left segment is

$$\tau_1 = R_1(sc_w + C_4) + sr_wC_4 + \frac{1}{2}r_wc_ws^2$$

and that of the right segment is

$$\tau_2 = R_4((L-s)c_w + C_2) + (L-s)r_wC_2 + \frac{1}{2}r_wc_w(L-s)^2$$

so the total delay is $\tau = \tau_1 + \tau_2$. To minimize τ,

$$\frac{d\tau}{ds} = 0 = (R_1c_w + r_wC_4 + r_wc_ws) + (-R_4c_w - r_wC_2 - r_wc_w(L-s))$$

$$s = \frac{1}{2}L - \frac{R_1 - R_4}{2r_w} - \frac{C_4 - C_2}{2c_w}$$