

**EE434**

**ASIC and Digital Systems**

**Final Exam**

**Apr. 30, 2018. (8am – 10am)**

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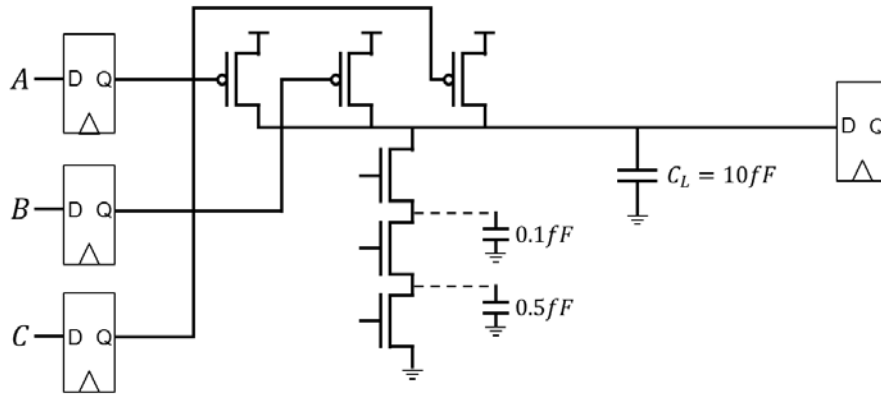
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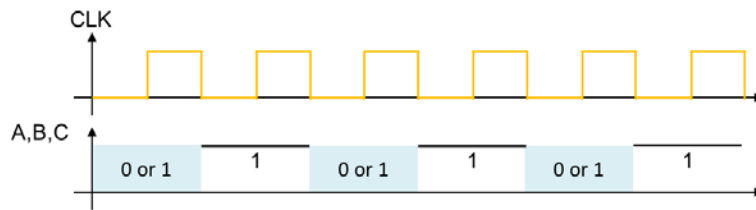
Problem	Points	
1	20	
2	10	
3	20	
4	20	
5	20	
6	20	
7	20	
8	20	
Total	150	

## Problem #1 (Logic Design, 20 points)

The following shows a three-input NAND gate surrounded by F/Fs.



The inputs (ABC) are generated from an input generator as follows:



In other words,  $ABC=(1,1,1)$  during even clock cycles and  $(0 \text{ or } 1, 0 \text{ or } 1, 0 \text{ or } 1)$  during odd clock cycles. The probabilities that A, B, and C become 0 or 1 during the odd clock cycles are as follows:

A: 0 (0.2), 1 (0.8)    B: 0 (0.3), 1 (0.7)    C: 0 (0.4), 1 (0.6)

Assign the input signals (the outputs of the F/Fs) to the gates of the three NFETs. You should minimize the total dynamic power consumption. The dynamic power is computed by  $\alpha f C V_{DD}^2$  where  $\alpha$  is the switching factor.

Since the output is always discharged during the even clock cycles, we can minimize the total dynamic power by minimizing the total capacitance charged during the odd clock cycles. For instance, if we assign ABC to the NFETs from the top, the expectation value will be

$$(0.8 \cdot 0.3 + 0.8 \cdot 0.7 \cdot 0.4) \cdot 0.1 \text{fF} + (0.8 \cdot 0.7 \cdot 0.4) \cdot 0.5 \text{fF} = 0.024 \text{fF} + 0.1344 \text{fF} = 0.1584 \text{fF}.$$

$$ABC: 0.8 \cdot 0.3 \cdot 0.1 \text{fF} + 0.8 \cdot 0.7 \cdot 0.4 \cdot 0.6 \text{fF} = 0.024 \text{fF} + 0.1344 \text{fF} = 0.1584 \text{fF}$$

$$ACB: (0.8 \cdot 0.4) \cdot 0.1 \text{fF} + (0.8 \cdot 0.6 \cdot 0.3) \cdot 0.6 \text{fF} = 0.032 \text{fF} + 0.0864 \text{fF} = 0.1184 \text{fF}$$

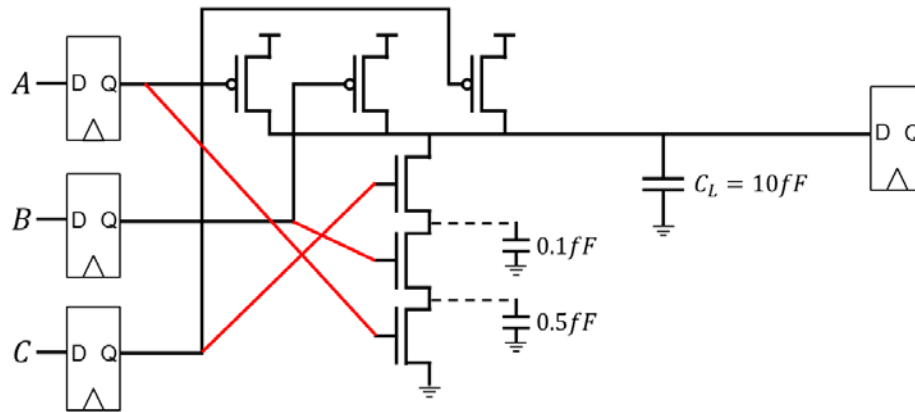
$$BAC: (0.7 \cdot 0.2) \cdot 0.1 \text{fF} + (0.7 \cdot 0.8 \cdot 0.4) \cdot 0.6 \text{fF} = 0.014 \text{fF} + 0.1344 \text{fF} = 0.1484 \text{fF}$$

$$\text{BCA: } (0.7 \cdot 0.4) \cdot 0.1 \text{fF} + (0.7 \cdot 0.6 \cdot 0.2) \cdot 0.6 \text{fF} = 0.028 \text{fF} + 0.0504 \text{fF} = 0.0784 \text{fF}$$

$$\text{CAB: } (0.6 \cdot 0.2) \cdot 0.1 \text{fF} + (0.6 \cdot 0.8 \cdot 0.3) \cdot 0.6 \text{fF} = 0.012 \text{fF} + 0.0864 \text{fF} = 0.0984 \text{fF}$$

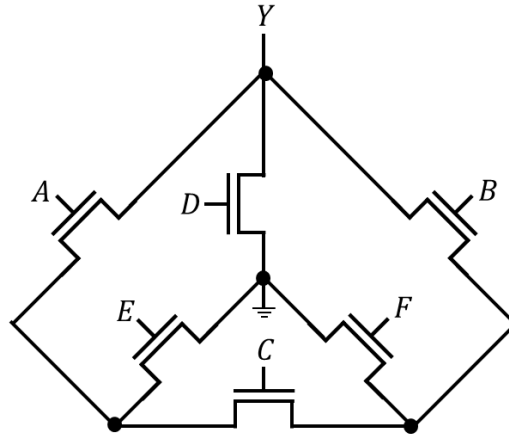
$$\text{CBA: } (0.6 \cdot 0.3) \cdot 0.1 \text{fF} + (0.6 \cdot 0.7 \cdot 0.2) \cdot 0.6 \text{fF} = 0.018 \text{fF} + 0.0504 \text{fF} = 0.0685 \text{fF}$$

Thus, CBA is the best assignment.



## Problem #2 (Logic Design, 10 points)

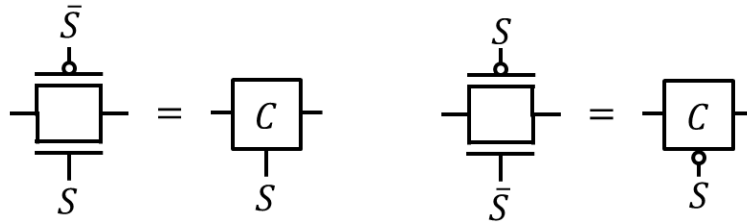
The following figure shows the NFET network of a static CMOS logic gate.  $Y$  is the output and  $A \sim F$  are the inputs of the gate. Express  $Y$  as a Boolean function of the inputs.



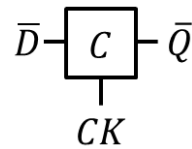
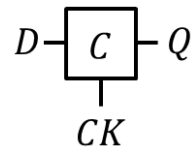
$$Y = \overline{D + AE + ACF + BF + BCE}$$

### Problem #3 (Logic Design, 20 points)

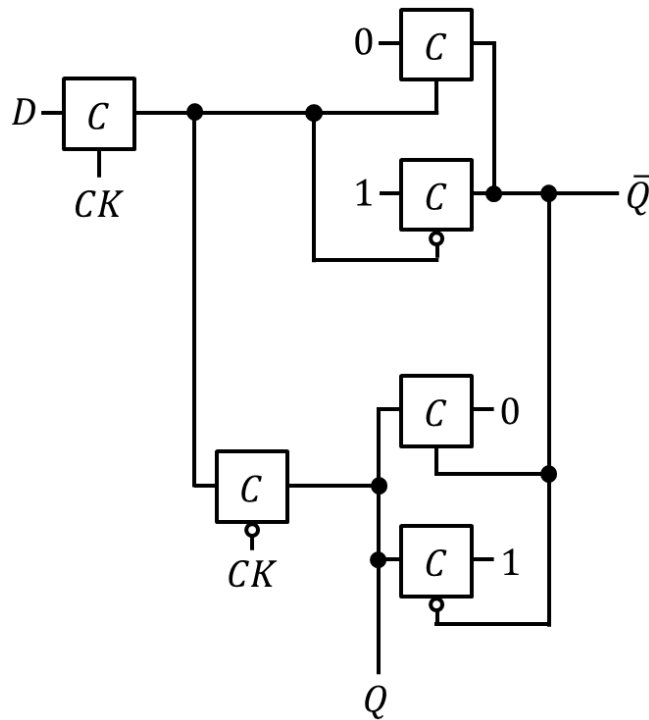
1) Design a positive D-latch (Q=D when CK=high, Q=hold when CK=low) using transmission gates only. Available inputs:  $D, \bar{D}, CK, \bar{CK}$ . Outputs:  $Q, \bar{Q}$ . You **cannot** use Power ( $V_{DD}$ ) and Ground ( $V_{SS}$ ). Use the following symbols for the transmission gates.



Try to minimize the # transmission gates.



2) Design a positive D-latch using transmission gates only. Available inputs:  $D, CK, \overline{CK}$ . Outputs:  $Q, \overline{Q}$ . You **can** use Power ( $V_{DD}$ ) and Ground ( $V_{SS}$ ) too. Try to minimize the # transmission gates.

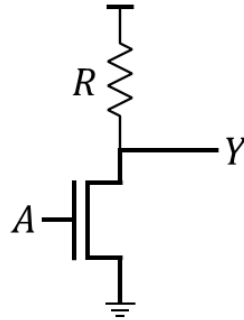


3) Does the D-latch design in Problem 1) have any problems? If yes, discuss the problems.

It will have a leakage or timing problem (the nodes driving Q and Q' are floating).

## Problem #4 (DC Characteristics, 20 points).

The following circuit shows an inverter design. When  $A$  is 0,  $Y$  is  $V_{DD}$ . When  $A$  is  $V_{DD}$ ,  $Y$  is close to 0. Sketch a DC characteristic curve for the inverter. You should split the curve into regions and show the operation mode of the NFET in each region. Express the output voltage  $V_Y$  as a function of  $R, V_A, V_{tn}, \beta_n, V_{DD}$  in each region.



- For the current in saturation mode, use  $I = \frac{1}{2}\beta_n(V_{GS} - V_{tn})^2$ .
- For the current in linear mode, use  $I = \beta_n \left\{ (V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2 \right\}$

### Region 1)

$$V_{GS} = V_A - 0 < V_{tn}: \text{Cut-off. } V_Y = V_{DD}$$

### Region 2)

$$V_{GS} > V_{tn} \text{ (ON)}$$

$$V_{DS} = V_Y - 0 \approx V_{DD} > V_{GS} - V_{tn} = V_A - V_{tn} \text{ (Saturation)}$$

$$\frac{V_{DD} - V_Y}{R} = \frac{1}{2}\beta_n(V_A - V_{tn})^2 \rightarrow V_Y = V_{DD} - \frac{R}{2}\beta_n(V_A - V_{tn})^2$$

### Region 3)

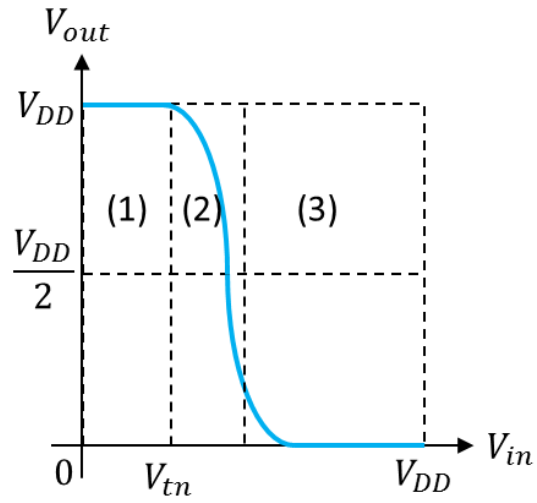
$$V_{GS} > V_{tn} \text{ (ON)}$$

$$V_{DS} = V_Y - 0 \approx 0 < V_{GS} - V_{tn} = V_A - V_{tn} \approx V_{DD} - V_{tn} \text{ (Linear)}$$

$$\frac{V_{DD} - V_Y}{R} = \beta_n \left\{ (V_A - V_{tn})V_Y - \frac{1}{2}V_Y^2 \right\} \rightarrow V_{DD} - V_Y = R\beta_n \left\{ (V_A - V_{tn})V_Y - \frac{1}{2}V_Y^2 \right\}$$

$$\rightarrow \frac{R\beta_n}{2}V_Y^2 - \{1 + R\beta_n(V_A - V_{tn})\}V_Y + V_{DD} = 0 \rightarrow$$

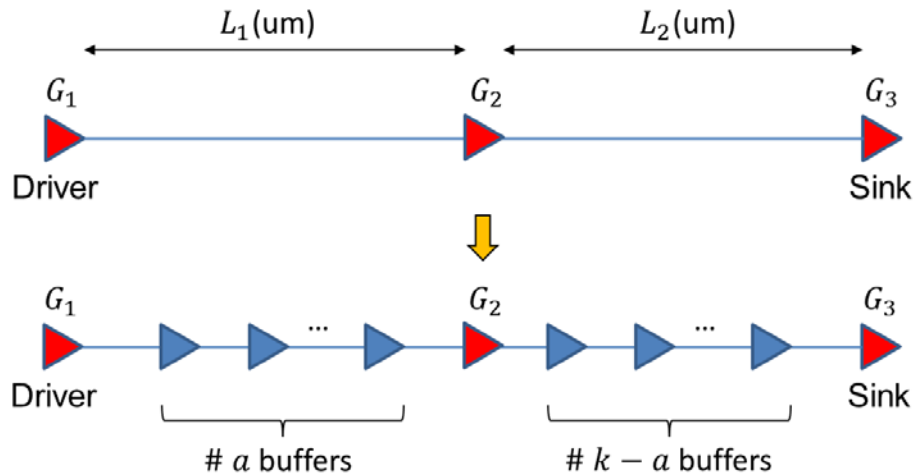
$$V_Y = \frac{\{1 + R\beta_n(V_A - V_{tn})\} - \sqrt{\{1 + R\beta_n(V_A - V_{tn})\}^2 - 2R\beta_n V_{DD}}}{R\beta_n}$$





## Problem #5 (Interconnects, 20 points)

The following shows two nets connecting three gates ( $G_1, G_2, G_3$ ). To reduce the delay, you insert buffers between  $G_1$  and  $G_2$  and between  $G_2$  and  $G_3$ . The total number of buffers you insert is  $k$  (constant). Thus, the total number of buffers you insert between  $G_1$  and  $G_2$  is  $a$  and the total number of buffers you insert between  $G_2$  and  $G_3$  is  $k - a$ . Find  $a$ , i.e., express  $a$  as a function of  $L_1, L_2, k$  minimizing the total delay (from  $G_1$  to  $G_3$ ).



- All the gates ( $G_1, G_2, G_3$ ) and the buffers are of the same type (i.e., they have the same output resistance, input capacitance, and internal delay).

We will use the fact that the buffers should be evenly distributed between  $G_1$  and  $G_2$  and between  $G_2$  and  $G_3$  because they are of the same type.

$$\text{Total delay } T = k\tau + (a + 1) \left( R \frac{L_1}{a+1} c + RC_{in} + r \frac{L_1}{a+1} C_{in} + \frac{1}{2} rc \left( \frac{L_1}{a+1} \right)^2 \right) + (k - a + 1) \left( R \frac{L_2}{k-a+1} c + RC_{in} + r \frac{L_2}{k-a+1} C_{in} + \frac{1}{2} rc \left( \frac{L_2}{k-a+1} \right)^2 \right)$$

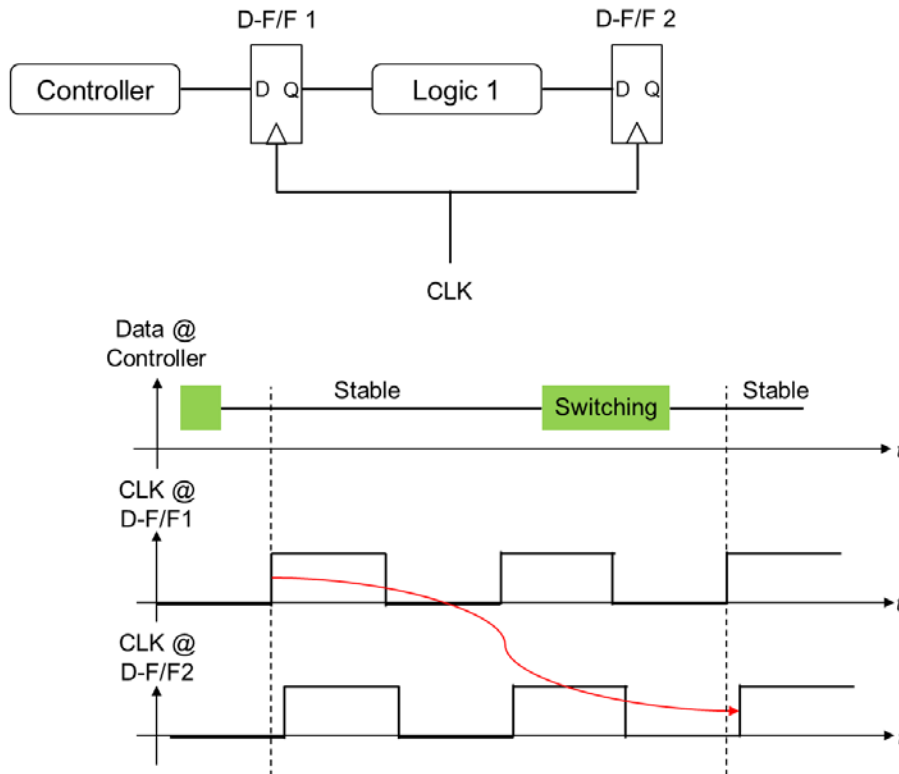
where  $\tau$  is the delay of each gate,  $r$  is the unit wire resistance,  $c$  is the unit wire capacitance,  $R$  is the output resistance of a gate, and  $C_{in}$  is the input capacitance of a gate.

$$\frac{dT}{da} = -\frac{1}{2} rc \left( \frac{L_1}{a+1} \right)^2 + \frac{1}{2} rc \left( \frac{L_2}{k-a+1} \right)^2 = 0$$

$$\frac{L_1}{a+1} = \frac{L_2}{k-a+1}$$

$$\therefore a = \frac{kL_1 + L_1 - L_2}{L_1 + L_2}$$

## Problem #6 (Timing Analysis, 20 points)



The figure shown above shows a multi-cycle logic. In general, a logic between two pipeline stages (or FFs) takes one clock cycle. If the logic delay is greater than the clock period, however, we can consider the logic a two-cycle logic, which takes two clock cycles. If a logic requires more than one clock cycle, it is called a multi-cycle logic. The waveform shows how the data captured by D-F/F 1 is computed and transferred to D-F/F 2 after two clock cycles. The controller logic guarantees that each data fed into Logic 1 through D-F/F 1 is held for two clock cycles.

Find a setup time and a hold time constraints for Logic 1 shown above. Use the following constants.

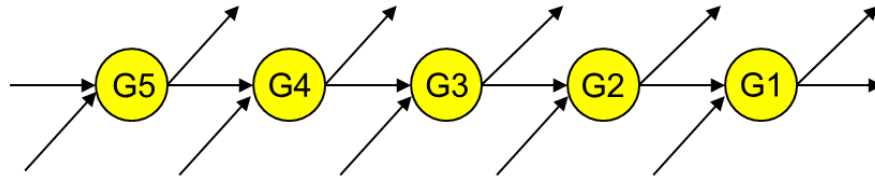
- For D-F/F 1
  - Setup time:  $s_1$ , Hold time:  $h_1$ , C-Q delay:  $C_1$
- For D-F/F 2
  - Setup time:  $s_2$ , Hold time:  $h_2$ , C-Q delay:  $C_2$
- Logic 1 delay:  $L_1$
- Clock period:  $T_{CK}$
- Delay from CLK to D-FF 1:  $D_1$
- Delay from CLK to D-FF 2:  $D_2$

Setup time:  $D_1 + C_1 + L_1 \leq D_2 + 2T_{CK} - s_2$

Hold time:  $D_1 + C_1 + L_1 \geq D_2 + h_2$

## Problem #7 (Timing Analysis, 20 points)

The following figure shows a general signal path. Assume that 1) each gate is combinational, 2) each gate has multiple input ports, 3) each gate has one output port, and 4) there is no feedback path in the circuit.  $G_i$  is the  $i$ -th combinational gate.



Suppose the slacks (= required time – arrival time) at the output ports of gate  $G_2$  and  $G_4$  are  $S_{G_2}$  and  $S_{G_4}$ , respectively. Prove or disprove that  $S_{G_4} < S_{G_2}$  is always satisfied.

False.

$$S_{G_2} = R_{G_2} - A_{G_2}$$

$$S_{G_4} = R_{G_4} - A_{G_4}$$

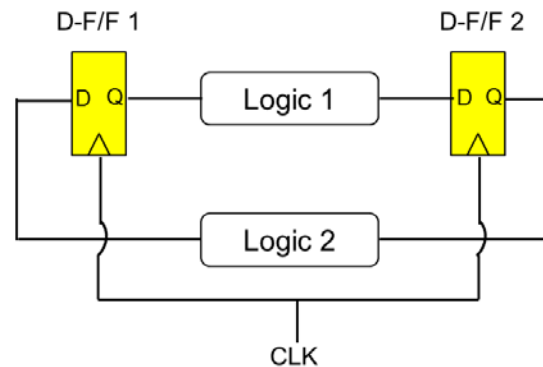
$$R_{G_4} < R_{G_2}$$

$$A_{G_4} < A_{G_2}$$

Thus, if  $A_{G_4}$  is very small but  $A_{G_2}$  is very large (due to some other signal paths coming to  $G_2$ ),  $S_{G_4} > S_{G_2}$  will be satisfied.

## Problem #8 (Timing Analysis, 20 points)

Find all setup and hold time constraints (inequalities) for the following system.



Use the followings for the constraints:

- Clock period:  $T_{CLK}$
- Delay from the clock source to the clock pin of D-F/F 1:  $D_1$
- Delay from the clock source to the clock pin of D-F/F 2:  $D_2$
- C-Q delay of D-F/F 1:  $C_1$
- C-Q delay of D-F/F 2:  $C_2$
- Delay of Logic 1:  $L_1$
- Delay of Logic 2:  $L_2$
- Setup time of D-F/F 1:  $S_1$
- Setup time of D-F/F 2:  $S_2$
- Hold time of D-F/F 1:  $H_1$
- Hold time of D-F/F 2:  $H_2$

For Logic 1

$$\text{(Setup time)} \quad D_1 + C_1 + L_1 \leq D_2 + T_{CLK} - S_2$$

$$\text{(Hold time)} \quad D_1 + C_1 + L_1 \geq D_2 + H_2$$

For Logic 2

$$\text{(Setup time)} \quad D_2 + C_2 + L_2 \leq D_1 + T_{CLK} - S_1$$

$$\text{(Hold time)} \quad D_2 + C_2 + L_2 \geq D_1 + H_1$$