EE434

ASIC and Digital Systems

Midterm Exam 2

April 8, 2015. (5:10pm – 6pm)

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Name:

WSU ID:

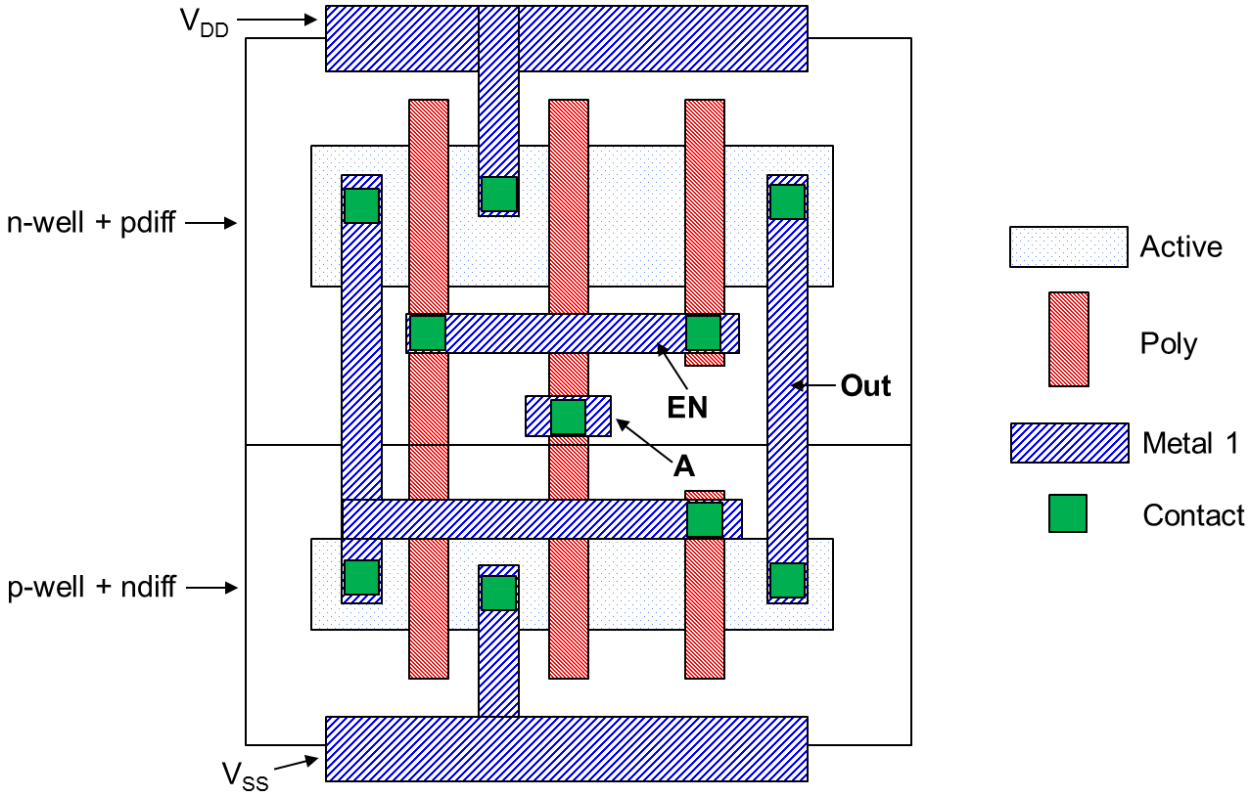
Problem	Points	
1	20	
2-1	13	
2-2	7	
3-1	10	
3-2	10	
4	20	
Total	80	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

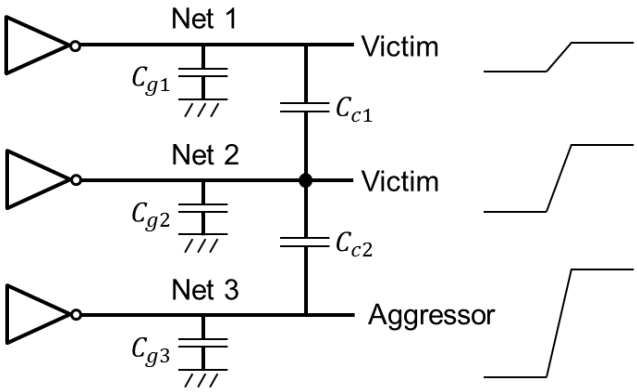
Problem #1 (Layout, 20 points).

Represent Out as a Boolean function of EN and A or describe the function of the following layout in as much detail as possible (Primary inputs: A, EN. Primary output: Out).

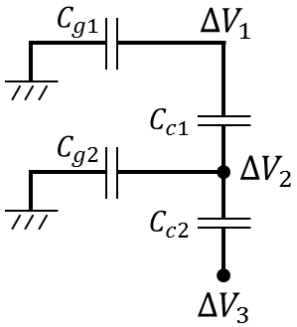


Problem #2 (Coupling Analysis, 20 points).

Three nets are coupled through C_{c1} and C_{c2} as shown in the following figure:



Net 3 is the only aggressor and Net 2 and Net 1 are victims. Although Net 1 is not directly connected to Net 3, Net 1 is affected by the potential change of Net 2 when Net 3 switches. The above figure can be simplified as follows:

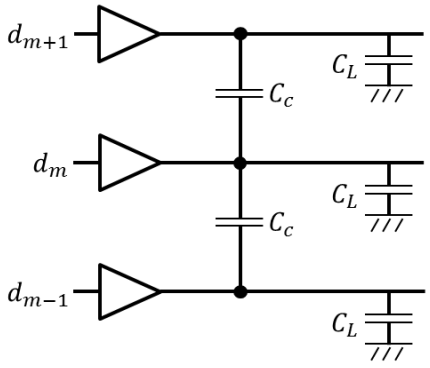


1 – 13 points) Derive ΔV_2 and ΔV_1 as a function of $\Delta V_3, C_{g1}, C_{g2}, C_{c1}$, and C_{c2}.

2 – 7 points) True/False questions (Hint: Use your intuition or the formulas you derived in the above problem).

a) If C_{g1} increases, ΔV_1 increases (true/false).
b) If C_{g1} increases, ΔV_2 increases (true/false).
c) If C_{g2} increases, ΔV_1 increases (true/false).
d) If C_{g2} increases, ΔV_2 increases (true/false).
e) If C_{c1} increases, ΔV_1 increases (true/false).
f) If C_{c2} increases, ΔV_1 increases (true/false).
g) If C_{c2} increases, ΔV_2 increases (true/false).

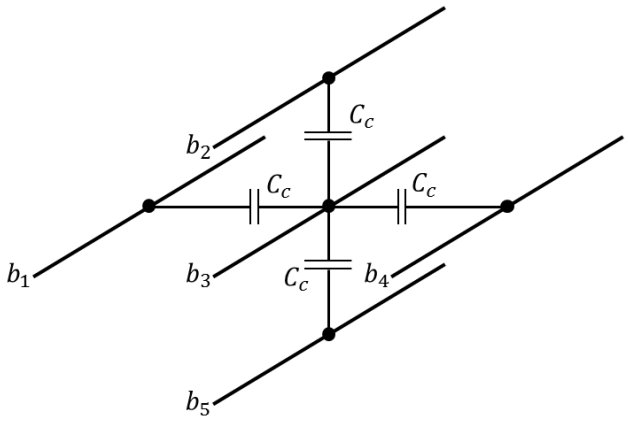
Problem #3 (Coupling Minimization, 20 points).



1 – 10 points) Compute effective capacitance for the net in the middle (d_m) for the following transition patterns:

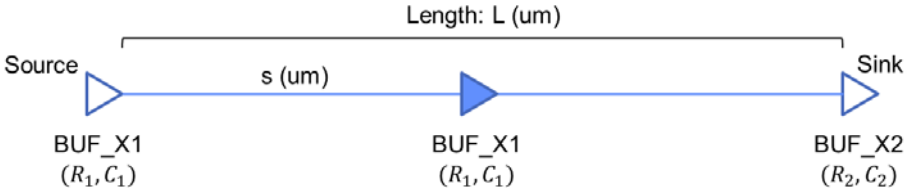
Transition patterns (d_{m+1} d_m d_{m-1})	Effective cap of d_m
010 → 000	
010 → 001	
010 → 100	
010 → 101	

2 – 10 points) A bus consisting of five bits (b_1 b_2 b_3 b_4 b_5) is routed in three metal layers. Due to some unknown reasons, four of them (b_1 b_2 b_4 b_5) are routed in parallel with b_3. The following shows the coupling capacitance among the five nets.



Due to the coupling between b_3 and b_k, the worst-case effective coupling capacitance that b_3 experiences will be $8 \cdot C_c$. List all transition patterns that make b_3 experience $8 \cdot C_c$ and $7 \cdot C_c$.

Problem #4 (Buffer Insertion, 20 points).



A source (type: BUF_X1) drives a sink (type: BUF_X2) through a net and you are supposed to insert a buffer (type: BUF_X1) between them as shown in the above figure. Find an optimal location of the buffer minimizing the total delay, i.e., represent “s” as a function of the following parameters.

- Output resistance of BUF_X1: R_1
- Input capacitance of BUF_X1: C_1
- Input capacitance of BUF_X2: C_2
- Total length of the net: L (um)
- Total wire resistance: R_w
- Total wire capacitance: C_w
- $(C_w + C_2 > C_1)$