EE434 ASIC & Digital Systems

Automatic Layout Generation (Cadence Innovus)

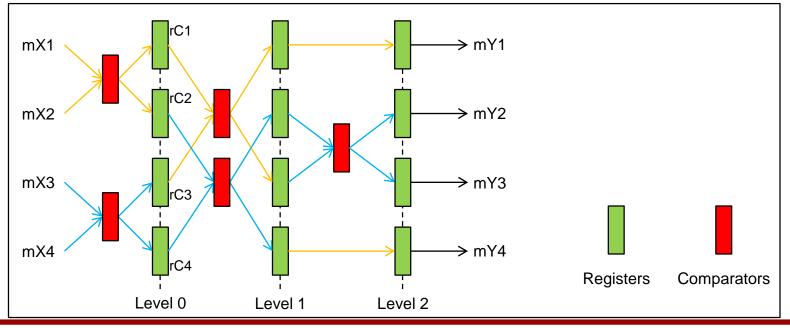
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Preparation for Lab2

- Download the following file into your working directory.
 wget http://eecs.wsu.edu/~ee434/Labs/lab2.tar.gz
- Unzip it.
 - tar xvfz lab2.tar.gz
- Before you run Innovus, you should source the following files:
 - source ictools_generic.sh
 - source cadence_innovus17.sh

Benchmark

- VQS64_4 (four-input 64-bit pipelined quick sort)
 - input [63:0] mX1, mX2, mX3, mX4
 - input mCLK
 - output [63:0] mY1, mY2, mY3, mY4



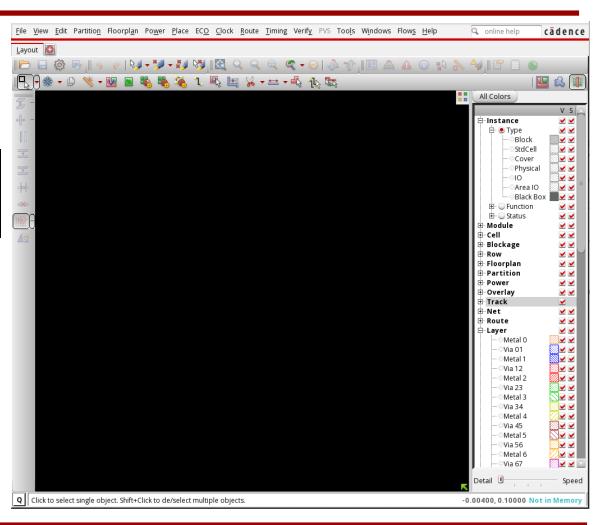
What We Are Going To Do

- 1. Chip outlining
- 2. P/G network design
- 3. Placement
- 4. Pre-CTS optimization
- 5. CTS
- 6. Post-CTS optimization
- 7. Routing
- 8. Post-routing optimization
- 9. Fill insertion

- Run Innovus.
 - innovus
- See the terminal.

**INFO:	MMMC	transition	support	version	v31-84
innovus innovus innovus	1>				

- You can use
 - GUI
 - Text commands



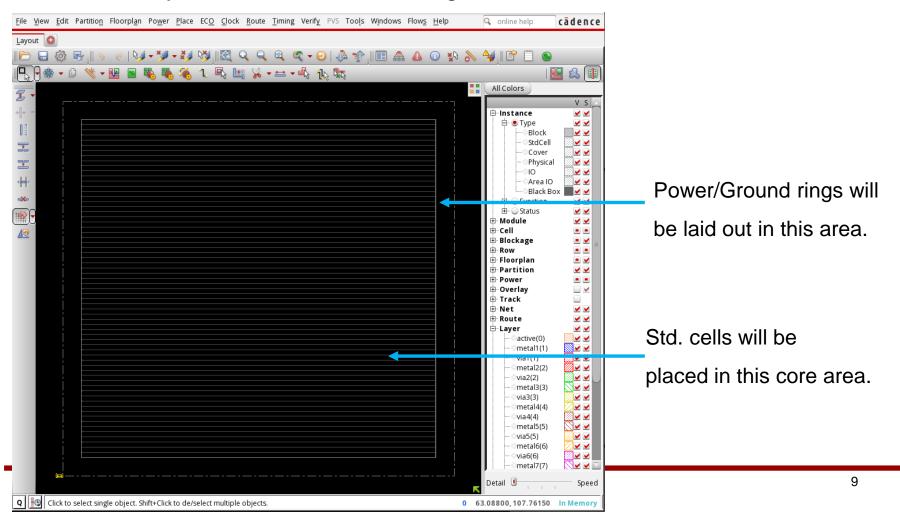
- Click "File" \rightarrow "Import Design...".
- In the "Design Import" window, click "Load..." and choose "VQS64_4_m.globals". This will automatically fill up the settings. Then, click "OK".

X Design Import	– 🗆 X	X Design Import —	
Netlist:			
 Verilog 		• Verilog	
Files:		Files: VQS64_4_fm.v	
	Top Cell: Auto Assign 🖲 By User:	Top Cell: Auto Assign 🔾 By User:	
O OA		O OA	
Library:		Library:	-
Cell:		Cell:	-
View:		View	•
Technology/Physical Libraries: –		Technology/Physical Libraries:	
• OA		○ OA	
Reference Libraries:		Reference Libraries:	
Abstract View Names:		Abstract View Names:	
Layout View Names:		Layout View Names:	
⊖ LEF Files		LEF Files lib/lef/NangateOpenCellLibrary.lef	
Floorplan		Floorplan	
IO Assignment File:		IO Assignment File:	6
Power		Power	
Power Nets:		Power Nets: VDD	
Ground Nets:		Ground Nets: VSS	
CPF File:	6	CPF File:	e
Analysis Configuration		Analysis Configuration	
MMMC View Definition File:		MMMC View Definition File: VQS64_4_fm.view	B
	Create Analysis Configuration	Create Analysis Configuration	
OK Save	Load Cancel Help	OK Save Load Cancel	<u>H</u> elp

- See the terminal for Innovus messages. There might be some Error or Warning messages. You can ignore them.
- In the Innovus main window, press "f" to see the outline of the layout.
- Innovus automatically computes and prepares the layout area.
- Let's modify the layout area.
- In the main window, click "Floorplan" \rightarrow "Specify Floorplan...".
- Set the core utilization to 0.6.
- Set the core-to-left, core-to-top, core-to-right, and core-to-bottom to 5.0.
- Then, click OK.

🗙 s	pecify Floorplan			- 0	×
Ba	asic Advanced				
۲	Design Dimensio	ns			
	Specify By: 🖲 Size	e 🔾 Die/IO/Core Coordinate	25		
	Core Size by:	 Aspect Ratio: 	Ratio (H/W):	345392877	
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			Cell Utilization:	0.699971	
		Oimension:	Width:	88.45	
			Height:	86.8	
	Oie Size by:		Width:	88.45	
			Height:	86.8	
	Core Margins b	y: 🥑 Core to IO Boundary			
		Core to Die Boundary			
		Core to Left: 5	Core to Top:	5	
		Core to Right: 5	Core to Bottom:	5	
	Die Size Calcula	ition Use: 🛛 🔾 Max IO He	ight 🖲 Min IO Heigh	it	- II.
	Floorplan Origi	n at: 💿 Lower Left	Corner 🔾 Center		
				Unit: Mic	ron
	<u>о</u> к	Apply	<u>C</u> ancel	<u>H</u> elp	

• Now, you will see the following window.



Save

- Let's save the current design.
- In the terminal, run the following command to save the current design into "test_01_floorplan.enc". innovus #> saveDesign test_01_floorplan.enc
- Later on, you can load the design as follows.
 - Run Innovus, click File → Restore Design → Data Type: Innovus → select the .enc file.

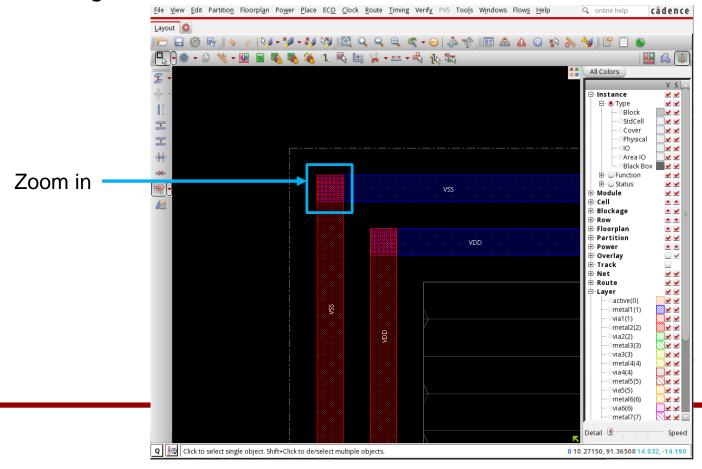
• Click "Power" \rightarrow "Power Planning" \rightarrow "Add Rings...".

X Add Rings		_		\times
Basic Advanced Via Generation Mo	de <u>P</u> review			
Net(s): VDD VSS				
Ring Type			, 	
Core ring(s) contouring				
Around core boundary 🕨 🗔 Exclud	e selected objects			
 Block ring(s) around 				
Each block >				
O User defined coordinates: Core ring				
Ring Configuration				
Layer: Width: Spacir	g: Offset:			
Top: metal1(1) H 🕨 1 1	1			
Bottom: metal1(1) H 🕨 1 1	1			
Left: metal2(2) V 🕨 1 1	1			
Right: metal2(2) V 🕨 1 1	1			
☑ Offset: Center in channel Upda	:e			
OK Apply	<u>D</u> efaults	<u>C</u> ancel	<u>H</u> elp	

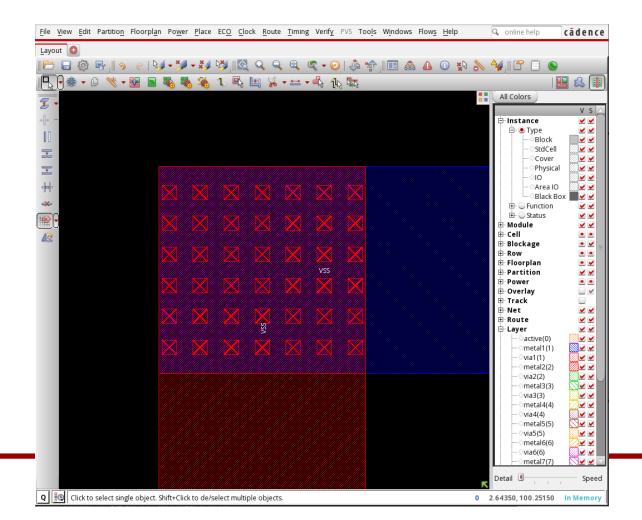
• Fill in the input boxes as shown in the previous page and click OK. Now you can see the power and ground rings.

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															@metal7(7)	

 Zoom in the top-left corner (Mouse right click – hold – drag – release). As shown below, the outer ring is VSS and the inner ring is VDD. Blue: Metal 1. Red: Metal 2. Zoom in the via arrays.



• The "X" squares are vias connecting the M1 and M2 wires.

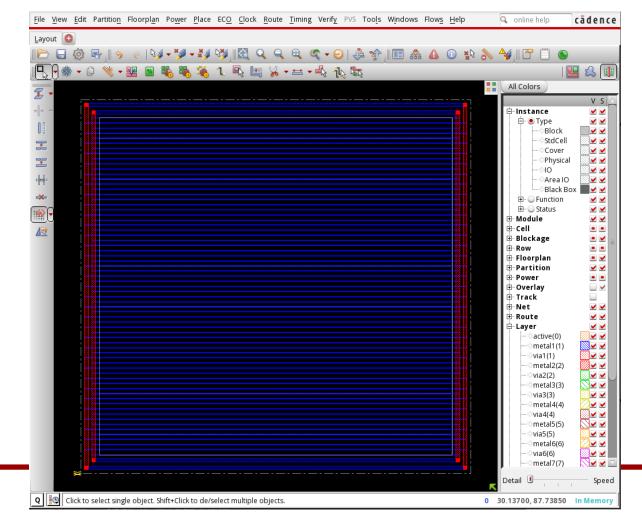


- Press "f" to zoom out to the full design.
- Now, we will draw power/ground stripes to connect the P/G rings to standard cells.

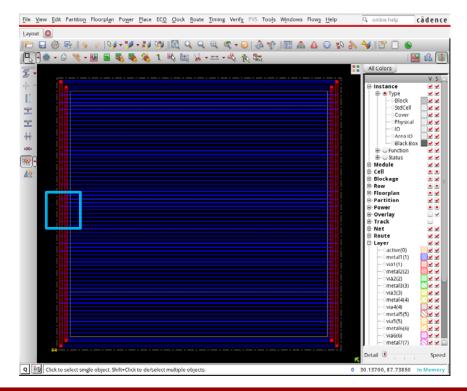
• Click "Route" → "Special Route...".

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sic Adva <u>n</u> ced <u>V</u> ia Generation				- 1
et(s): VDD VSS	<u></u>			
Route				
🕑 Block Pins 🗹 Pad Rings 🛛 🗹 Floating Stripes				
Pad Pins Verlow Pins Secondary Power Pins				
outing Control				ΞI
Layer Change Control				ЪШ
Top Layer: metal10(10) Bottom Layer: metal1(1)				
Allow Jogging 🛛 🗹 Allow Layer Change				
Specify Area				
X1: Y1:				
X2: Y2:				
Connect to Target Inside The Area Only				
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● All ○ Selected				
O Named:				
🔄 Delete Existing Routes 🛛 📃 Generate Progress Messages				
ode Setup	Target	Editing	g Option	s
	_ 0		5 - 1	

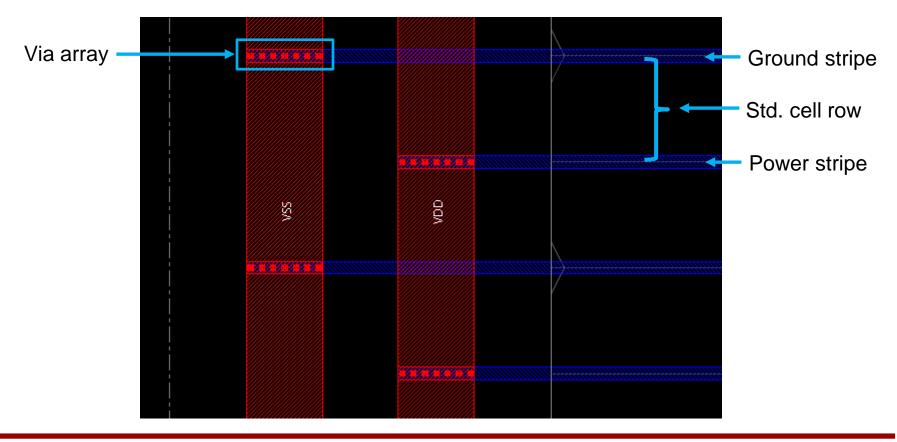
• P/G network



- saveDesign test_02_pg.enc
- Zoom in the following area.



 As you see, the P/G stripes are alternating between VDD and VSS. See the vias.



- Let's place the instances (cells).
- In the main window, click "Place" \rightarrow "Place Standard Cell".
- In the "Place" window, click "Mode".

🔀 Place	-		×							
💿 Run Full Placement 🔾 Run Incremental Placement 🔾 Run Placement In Floorplan Mode										
Optimization Options										
Include Pre-Place Optimization	✓ Include Pre-Place Optimization									
Number of Local CPU(s): 1 Set Multiple CPU										
OK <u>Apply Mode</u> <u>D</u> efaults <u>C</u> an	cel	<u>H</u> elp								

• Turn on "Place IO Pins". Set the "Specify Maximum Routing Layer" to 6. We will use only six metal layers. Click OK. In the "Place" window, click OK.

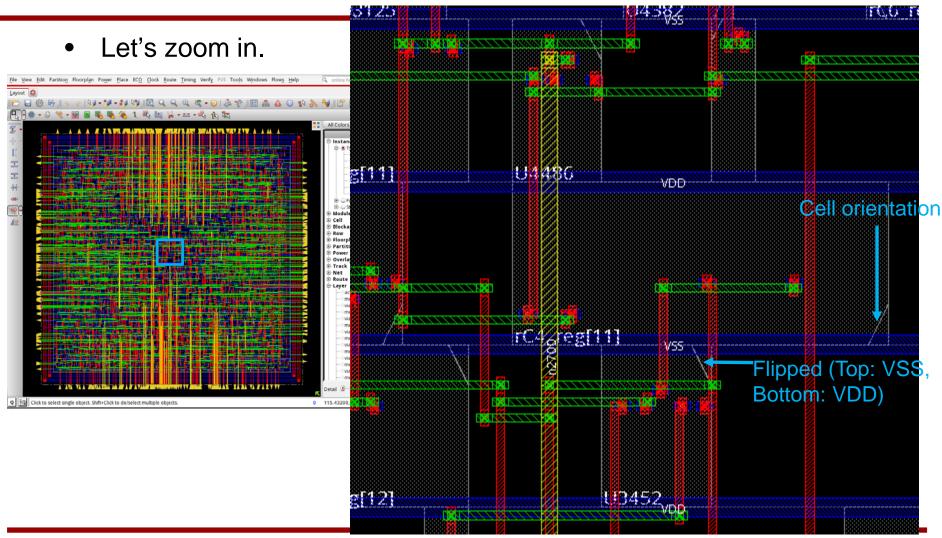
X Mode Setup		-		\times
List of Modes —	Placement Mode			
СТБ	Placement RefinePlace			
EarlyGlobalRoute EndCap Filler	 Congestion Effort Low Medium High Auto 			
NanoRoute OasisOut	🔾 Run Placement In FloorPlan Mode			
Optimization	Run Timing Driven Placement			
Placement	Enable Module Plan			
ScanReorder	Enable Clock Gating Awareness			
StreamOut	Enable Power Driven			
TieHiLo	☑ Ignore Scan Connections			
	☑ Reorder Scan Connection			
	Ignore Spare Cell Connections			
	☑ Place IO Pins			
	Hierarchy Aware Spare Cell Placement			
	Specify Maximum Density			
	Layers Checked For Pin Access	Select)	
	Specify Maximum Routing Layer 6			-
	Set Defaults			
<u></u>	Apply <u>C</u> ancel	<u>H</u> elp)	

- It shows placement and trialRoute results. trialRoute is just a quick routing for an estimation of some design metrics.
- See the terminal. It shows some more information. Click this button if you can't see the layout.
 - Total wire length: 32,540.21um

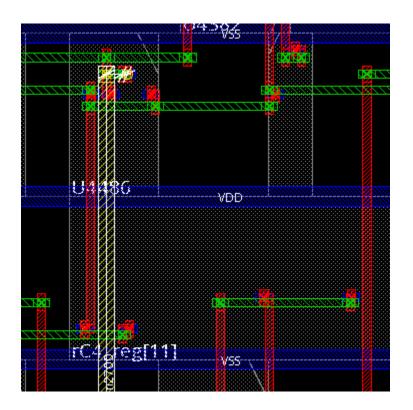
	ngth: 0.000000e+00um,		
	ngth: 1.563008e+04um,		
	ngth: 1.402659e+04um,		
	ngth: 1.713939e+03um,		
	ngth: 8.258645e+02um,		
Laver6(metal6)(V) ler	nath: 3.437350e+02um,	<u>number of</u> vias:	19
Total length: 3.25402	2le+04um, number of vi	ias: 22181	
			

- Save it.
 - saveDesign test_03_pl.enc

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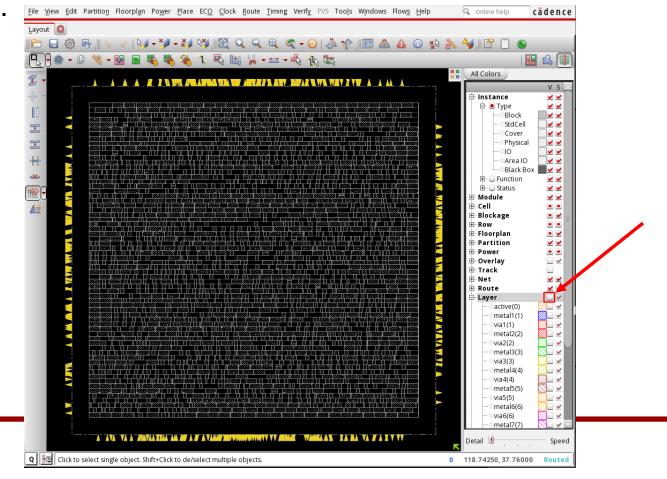
• Click a wire and press 'q'. You will see a property window.



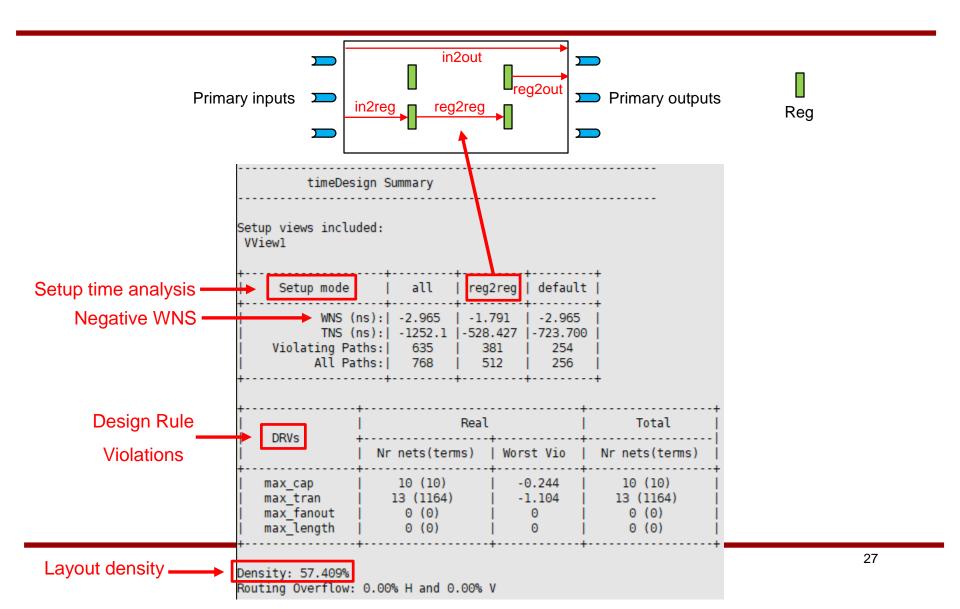
X Attrib	oute Editor	-		×					
Object Type: Regular Wire									
Name	Name Value T								
	Net Name	n2700	String						
	Wire Direction	dbcWireN >	Enumerat	e					
	Bounding Box	{45.945 31.22} {46.085 56.56}	Box						
	Routing Layer	metal4(4) >	Layer						
	Wire Status	Unknown 🕨	Enumerat	e					
	Rule	default 🕨	Enumerat	e					
	Mask	0	Integer						
1									
<u>о</u> к	<u>A</u> pply	Add Prop Delete Prop <u>C</u> lose	<u>H</u> elp						

Visibility

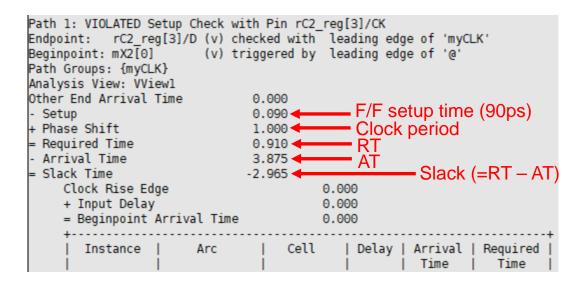
- Let's see the placement result only.
- Turn off the following check-box to turn off the visibility of the wires. Elle View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Cadence



- Run the following command to turn off SI-awareness.
 innovus #> setDelayCalMode –siAware false
- Then, run the following command to analyze setup time.
 - innovus #> timeDesign –preCTS
 - preCTS means "before Clock-Tree-Synthesis". A clock tree is designed after placement.
- It will show the following summary:



- Run the following command to check the longest path.
 - innovus #> report_timing
 - The clock frequency is 1GHz.



4. Pre-CTS Optimization

- Now, since the design violates the timing constraints, let's optimize it. (Notice that we can still try to optimize it to reduce power even if it satisfies the timing constraints.)
- Run the following command to optimize the design before CTS.
 innovus #> optDesign –preCTS
- (This will take some time, up to several minutes depending on the machine you are working with).
- After Pre-CTS optimization is done, you will see the following result:

4. Pre-CTS Optimization

• Pre-CTS optimization

	optDesign Final Summary								
	Setup views included: VViewl								
	Setup mode		all	reg	2reg default		-+		
Positive WNS!!! —	WNS (ns WNS (ns NS (ns Violating Path All Path		s): 0.000 0.00 hs: 0 0		003 000 0 12	0.001 0.000 0 256	 -+		
	++	Real					Total	-+	
	DRVs +	+ Nr nets(terms)			Worst Vio		Nr nets(terms)		
	max_cap max_tran max_fanout max_length +		0 (0) 0 (0) 0 (0) 0 (0)			.000 .000 0 0	0 (0) 0 (0) 0 (0) 0 (0) 0 (0)	-+ 	
	Density: 61.022%					ncrease	ed from 57% to	61%.	

4. Pre-CTS Optimization

• saveDesign test_04_prectsopt.enc

5. Clock Tree Synthesis (CTS)

- Run the following command to run CTS.
 - innovus #> create_ccopt_clock_tree_spec
 - innovus #> get_ccopt_clock_trees *
 - myCLK (You will see this.)
 - innovus #> set_ccopt_property_target_max_trans_0.05
 - Max. transition time at a clock pin is 50ps.
 - innovus #> set_ccopt_property_target_skew_0.02
 - Clock skew is 20ps.
 - innovus #> ccopt_design

5. Clock Tree Synthesis (CTS)

• saveDesign test_05_cts.enc

- Run the following command to check timing.
 - timeDesign -postCTS

optDesign Final Summary							timeDesign Summary							
Setup views inclu VViewl	ded:							etup views includ VViewl	led:					
+ Setup mode	+	all	reg2	reg	default	-+	+	Setup mode		all	+ reg2	reg	default	-+
WNS (ns): 0.001 0.003 TNS (ns): 0.000 0.000 Violating Paths: 0 0 All Paths: 768 512		00 	0.001 0.000 0 256		+	WNS (ns): TNS (ns): Violating Paths: All Paths:		0.000 0	0.0 0.0 0.0	000	0.011 0.000 0 256	-+ 		
+ 	+ 		Real		· · · · · · · · · · · · · · · · · · ·	-+ + Total	+				Real		+- 	-+ Total
DRVs 	Nr	Nr nets(terms)		Worst Vio		Nr nets(terms)		DRVs +		Nr nets(terms) Worst		st Vio	Nr nets(terms)	
/ max_cap max_tran max_fanout max_length		0 (0) 0 (0) 0 (0) 0 (0)		0.	000 000 0	0 (0) 0 (0) 0 (0) 0 (0)	+	max_cap max_tran max_fanout max_length		0 (0) 0 (0) 0 (0) 0 (0)		0.	000 000 0 0	0 (0) 0 (0) 0 (0) 0 (0)
+ Density: 61.022% Routing Overtiow:	+	% H and O.	.00% V			+		ensity: 61.239% outing Overtiow:	0.00	% H and O	.00% V	,	+	

6. Post-CTS Optimization

- Although we already satisfied the timing without any further optimization after CTS, we will run post-CTS optimization.
 - innovus #> optDesign –postCTS

optDesign Final Summary											
Setup views includ VViewl	ded:										
Setup mode all reg2reg default											
WNS (r TNS (r Violating Pat All Pat	ns): 0.000 ths: 0	: 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0		0.010 0.000 0 256							
 DRVs -		Real			Total						
	Nr nets(ter	ms)	Worst Vio		Nr nets(terms)						
max_cap max_tran max_fanout max_length	0 (0) 0 (0) 0 (0) 0 (0)		0.000 0.000 0		0 (0) 0 (0) 0 (0) 0 (0)						

Density: 61.239% Routing Overflow: 0.00% H and 0.00% V

6. Post-CTS Optimization

- saveDesign test_06_postctsopt.enc
- So far, we have done
 - Placement
 - CTS
- Now we will route the nets.

7. Routing

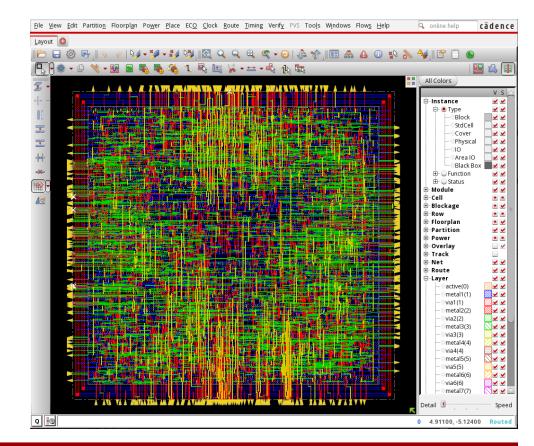
- Click "Route" \rightarrow "NanoRoute" \rightarrow "Route...".
- Make sure that the top layer is "6". If not, set it to 6.
- Click OK.

🗙 NanoRoute	-		×
Routing Phase Global Route Cotail Route Start Ite	eration default		
	Optimize Via D Optimize Wire		
Concurrent Routing F	eatures		
⊻ Fix Antenna	🔄 Insert Diodes Diode Cell Name		
Timing Driven	Effort 5 Congestion Timing S.M.A.R.T.		
SI Driven			
Post Route SI	SI Victim File 🖻		
Litho Driven			
🔄 Post Route Litho Repa	ir		
Routing Control			
Selected Nets Only	Bottom Layer default Top Layer 6		
ECO Route			
Area Route	Area Select Area and	Route	
Job Control			
🗹 Auto Stop			
	of Local CPU(s): 1		
Number of CPU(s) per Re			
Number of Rem Set Multiple CPU	ote Machine(s): 0		

7. Routing

- Routing result.
- See the log.
 - WL: 35,172um

```
#Post Route wire spread is done.
#Total number of nets with non-default rule or having
#Total wire length = 35172 um.
#Total half perimeter of net bounding box = 31277 um.
#Total wire length on LAYER metall = 1730 um.
#Total wire length on LAYER metal2 = 14515 um.
#Total wire length on LAYER metal3 = 13908 um.
#Total wire length on LAYER metal4 = 3849 um.
#Total wire length on LAYER metal5 = 998 um.
#Total wire length on LAYER metal6 = 173 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 20085
#Up-Via Summary (total 20085):
```



7. Routing

• saveDesign test_07_route.enc

- Run the following command to check timing.
 - timeDesign -postRoute

timeDesi	ign Su	mmary									
Setup views included: VViewl											
+ Setup mode	++ Setup mode all reg2reg default										
TNS (r Violating Pat	ns): ths:	0.014 0.000 0 768				-+					
+											
DRVs -	Nr	nets(tem	ns)	Worst Vio		Nr nets(terms)					
max_cap max_tran max_fanout max_length		0 (0) 0 (0) 0 (0) 0 (0)		0.000 0.000 0 0		0 (0) 0 (0) 0 (0) 0 (0)					
+ Density: 61.239%					+						

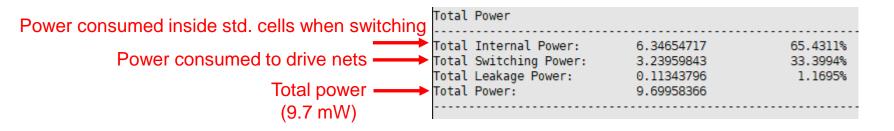
8. Post-Routing Optimization

- Although we've already satisfied the timing without any further optimization after routing, we will run post-routing optimization.
 - innovus #> optDesign _postRoute

optDesign Fin	nal Non-SI Timi	ng Summary		timeDe	timeDesign Summary						
Setup views inclu VViewl	ded:			Setup views incl VViewl	uded:						
+ Setup mode	all	reg2reg def	+ ault	+Setup mode	all re	g2reg default	-+ :				
WNS (n TNS (n Violating Pa All Pa	ns): 0.000 ths: 0	0.000 0.	013 000 0 56	TNS Violating P	(ns): 0.000 0 aths: 0	.019 0.014 .000 0.000 0 0 512 256	 				
+ DRVs	+ 	Real	Total	+ +	l Rea	l	Total				
	Nr nets(term	s) Worst Vi	o Nr nets(terms)	DRVs +	Nr nets(terms)	Worst Vio	Nr nets(terms)				
max_cap max_tran max_fanout max_length	0 (0) 0 (0) 0 (0) 0 (0)	0.000 0.000 0 0	0 (0) 0 (0) 0 (0) 0 (0)	max_cap max_tran max_fanout max_length + +	0 (0) 0 (0) 0 (0) 0 (0)	0.000 0.000 0 0	0 (0) 0 (0) 0 (0) 0 (0)				
Density: 61.239%				Density: 61.239%	i						
l	Before pos	stRoute o	pt.		After postR	oute opt.	41				

Power Analysis

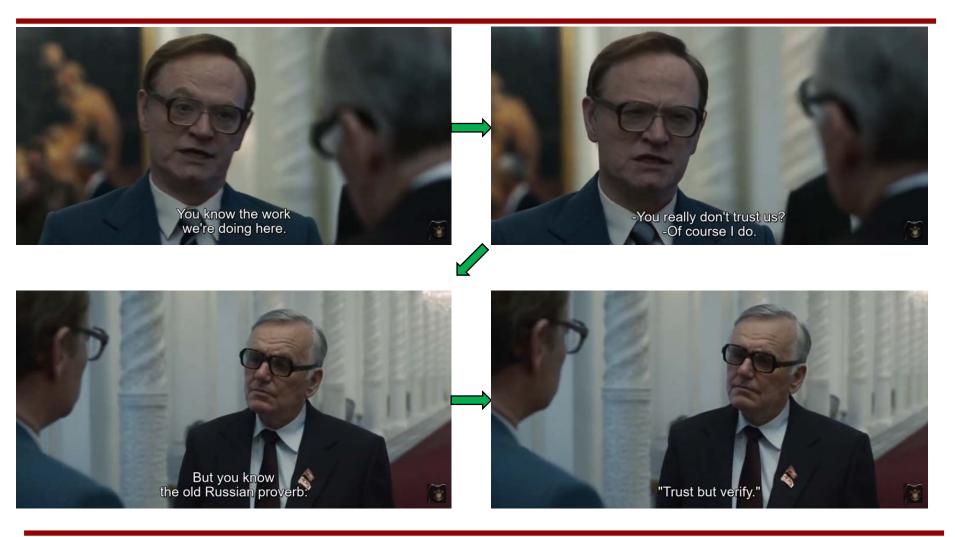
innovus #> report_power



8. Post-Routing Optimization

- saveDesign test_08_postrouteopt.enc
- Done.

9. Verification



9. Verification

• In the main menu, Verify \rightarrow Very Geometry. Click OK.

innovus 28> *** Starting Verify Geometry (MEM: 1346.7) *** **WARN: (IMPVFG-257): verifyGeometry command is replaced by verify drc command. It still works in this release but will be removed in future release. Please update your script to use the new command. VERIFY GEOMETRY Starting Verification VERIFY GEOMETRY Initializing VERIFY GEOMETRY Deleting Existing Violations VERIFY GEOMETRY Creating Sub-Areas bin size: 2160 VERIFY GEOMETRY SubArea : 1 of 1 **WARN: (IMPVFG-47): This warning message means the PG pin of macro/macros is not connected to relevant PG net in the design. If we q uery the particular PG pin 'net:NULL' will be displayed in the Innovus GUI. VERIFY GEOMETRY Cells : O Viols. VERIFY GEOMETRY SameNet : O Viols. VERIFY GEOMETRY Wiring : 6 Viols. VERIFY GEOMETRY Antenna : 0 Viols. VERIFY GEOMETRY Sub-Area : 1 complete 6 Viols. 0 Wrngs. VG: elapsed time: 1.00 Begin Summary ... Cells : 0 SameNet : 0 Wiring : 3 Antenna : 0 : 3 Short Overlap : 0 End Summary

9. Verification

• In the main menu, Verify \rightarrow Very Connectivity. Click OK.

innovus 28> innovus 28> VERIFY_CONNECTIVITY use new engine.
******* Start: VERIFY CONNECTIVITY *******
Start Time: Sun Mar 29 15:08:03 2020
Design Name: VQS64_4
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (107.1000, 102.4800)
Error Limit = 1000; Warning Limit = 50
Check all nets
Begin Summary
Found no problems or warnings.
End Summary
End Time: Sun Mar 29 15:08:03 2020
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ******* Verification Complete : 0 Viols. 0 Wrngs.

10. Conclusion

• Although there were six geometry violations, we will stop at this point.