EE434

ASIC and Digital Systems

Midterm Exam 1

February 25, 2015. (5:10pm – 6pm)

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Name:

WSU ID:

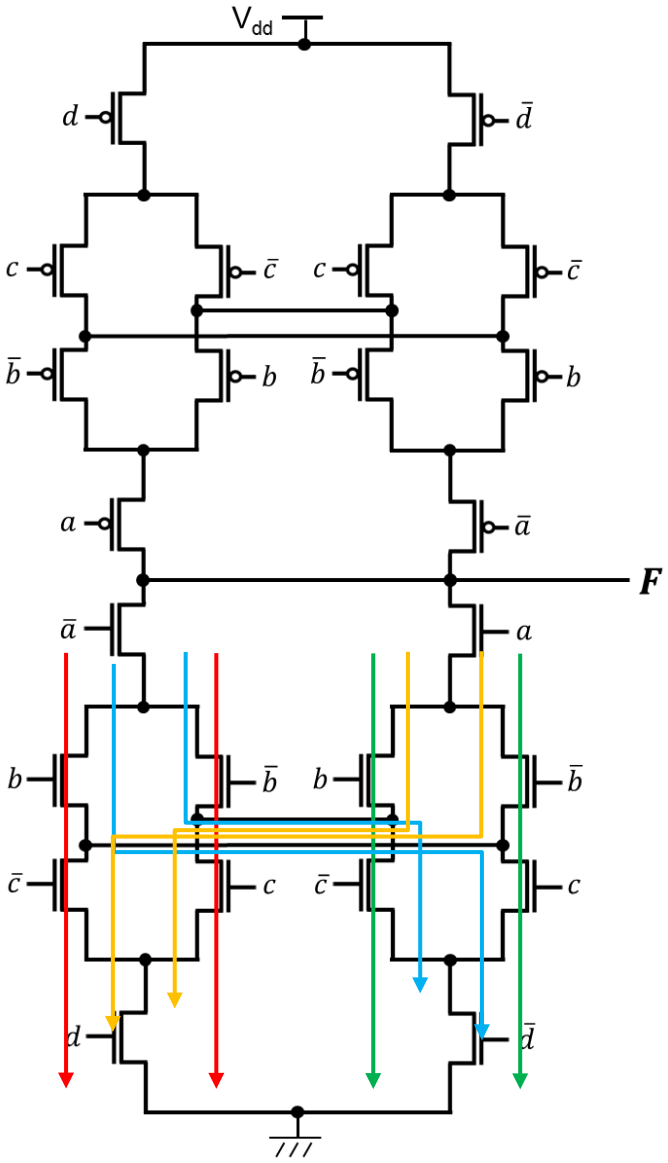
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
Total	80	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Static CMOS gates, 10 points).

Represent F as a function of $a, b, c,$ and d.

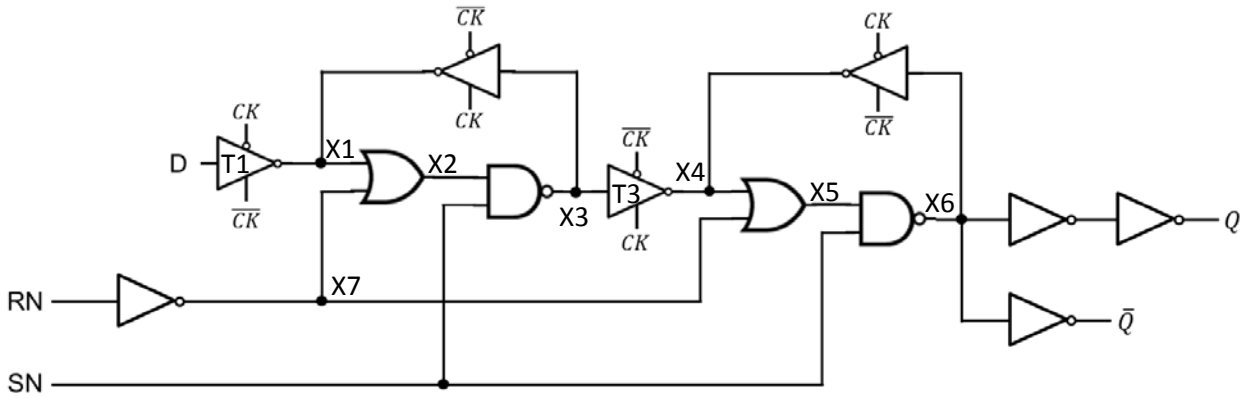


$$\bar{F} = \underline{\bar{a}d(b\bar{c} + \bar{b}c)} + \underline{a\bar{d}(b\bar{c} + \bar{b}c)} + \underline{\bar{a}\bar{d}(bc + \bar{b}\bar{c})} + \underline{ad(bc + \bar{b}\bar{c})}$$
$$= (\bar{a}d + a\bar{d})(b\bar{c} + \bar{b}c) + (\bar{a}\bar{d} + ad)(bc + \bar{b}\bar{c})$$
$$= (a \oplus d)(b \oplus c) + \overline{(a \oplus d)(b \oplus c)}$$
$$= \overline{(a \oplus d) \oplus (b \oplus c)}$$

$$\therefore F = a \oplus b \oplus c \oplus d$$

Problem #2 (Static CMOS gates, 10 points).

What does the following circuit do? Describe the function of the circuit in as much detail as possible.



1. SN=0 → X6=1 → Q=1: SN is an active-low asynchronous set.

2. SN=1, RN=0 → X7=1 → X5=1 → X6=0 → Q=0: RN is an active-low synchronous reset.

3. SN=1, RN=1 → X7=0

If CK=0 → T3 is off → Q=X6, X4=$\overline{X6}$, X5=X4, X6=$\overline{X5}$=$\overline{X4}$=X6 → $Q^+ = Q$

If CK=1 → T1 is off, T1 captures D, X1=$\overline{D}$ → X2=$\overline{D}$ → X3=D

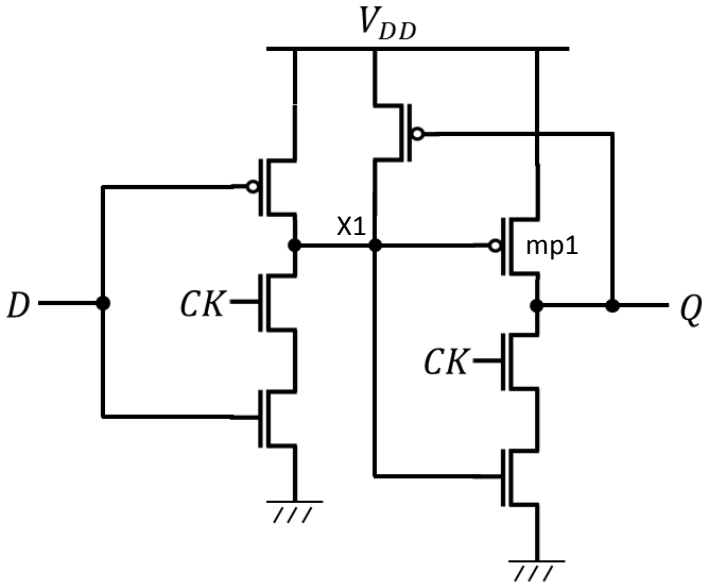
T3 is ON, X4=$\overline{X3}$=$\overline{D}$ → X5=X4 → X6=$\overline{X5}$=D → $Q^+ = D$

→ If SN=1 and RN=1, the circuit is just a positive edge-triggered D FF.

so, this is a positive edge-triggered D-FF with asynchronous active-low set and reset signals (set dominates reset).

Problem #3 (CMOS Logic, 10 points).

What is the functionality of the following circuit? Describe the functionality in as much detail as possible.



CK=1 → X1=$\overline{D}$ → Q=$\overline{X1}$=D

If D=0 → X1=1 → Q=0 → X1=1 (no conflict)

If D=1 → X1=0 → Q=1

CK=0 → The PDN of the right half is off.

If D=0 → X1=1 → mp1 is off → Q is floating (hold)

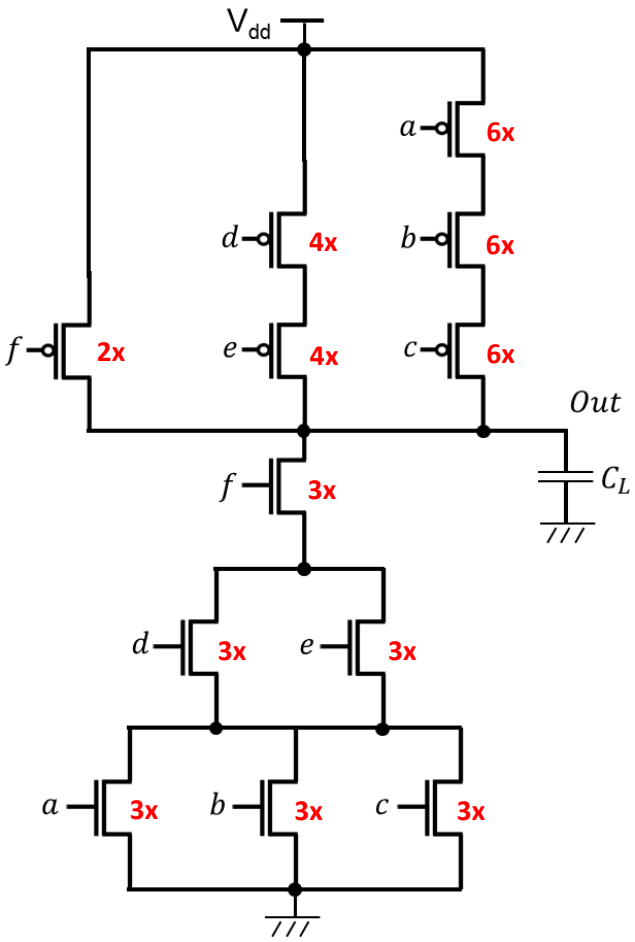
If D=1, Q=0 → X1=1 → mp1 is off → Q is floating (hold)

If D=1, Q=1 → X1 is floating (hold) → Q is floating (hold)

so, this is a **tri-state D-latch**.

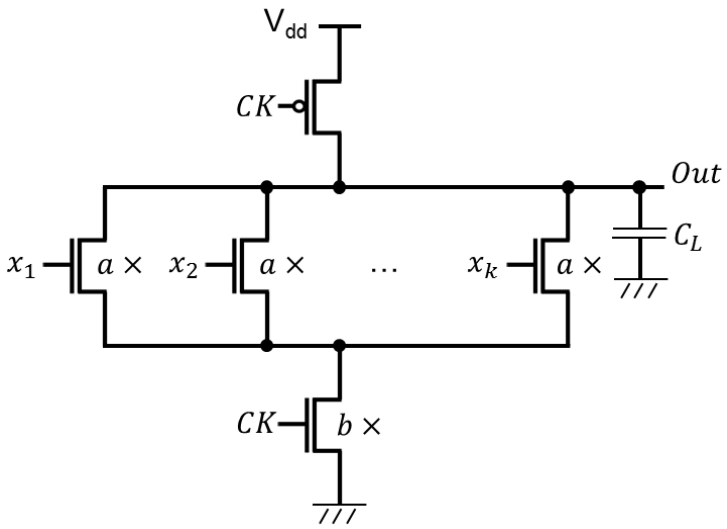
Problem #4 (Transistor Sizing, 10 points).

Size the transistors in the following gate. R_n is the resistance of a 1X NMOS transistor. $\mu_n = 2 \cdot \mu_p$. Ignore all the parasitic capacitances. Target time constant: $\tau_{target} = R_n \cdot C_L$. Try to minimize the total area.



Problem #5 (Transistor Sizing, 10 points).

We want to design a *k*-input NOR gate. However, the static CMOS gate design methodology is not suitable for the design of the *k*-input NOR gate due to area overhead in the pull-up network and the body-bias effect. Therefore, we are going to design it using the dynamic CMOS design methodology. The following shows a schematic of the *k*-input NOR gate.



R_n is the resistance of a 1X NMOS transistor. $\mu_n = 2 \cdot \mu_p$. Ignore all the parasitic capacitances. Target time constant: $\tau_{target} = R_n \cdot C_L$. All the transistors for $x_1 \sim x_k$ are upsized to aX and the transistor for CK is upsized to bX (a and b are ***real*** numbers). We ***minimize*** the total width, $Width = a \cdot k + b$. Find a and b (i.e., derive a (and b) as a function of k) minimizing the total width.

Constraint: $\left(\frac{R_n}{a} + \frac{R_n}{b}\right) C_L = R_n C_L \Rightarrow \frac{1}{a} + \frac{1}{b} = 1$

$W = ak + b = ak + \frac{a}{a-1}$

1) $W' = k + \frac{(a-1)-a}{(a-1)^2} = k - \frac{1}{(a-1)^2} = 0 \Rightarrow \boxed{a = 1 + \frac{1}{\sqrt{k}} \Rightarrow b = 1 + \sqrt{k}}$

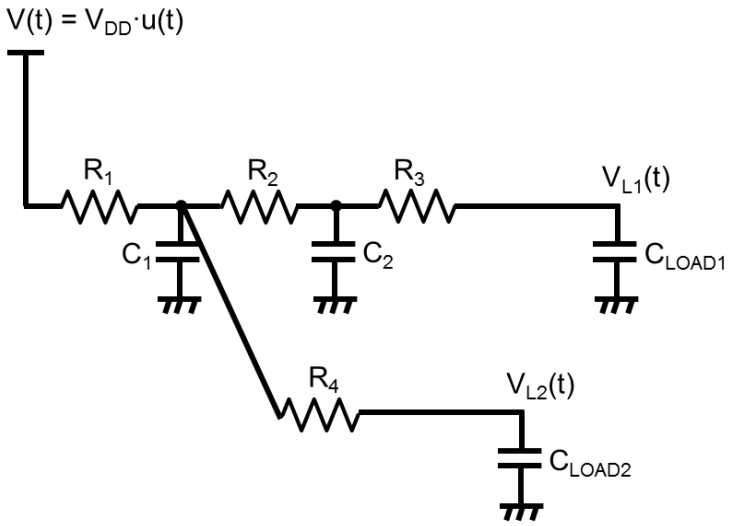
2) $ak + b = c$ => Two functions, $b = -ak + c$ and $b = \frac{a}{a-1}$, should meet at a single point (confirm this by drawing their graphs).

$\Rightarrow -ak + c = \frac{a}{a-1}$ should have a single root. $\Rightarrow ka^2 - (k + c - 1)a + c = 0$ has a single root. $\Rightarrow (k + c - 1)^2 - 4kc = 0 \Rightarrow (k - c - 1)^2 = 0 \Rightarrow c = k + 1 \pm 2\sqrt{k} \Rightarrow$

$a = 1 \pm \frac{1}{\sqrt{k}} \Rightarrow a > 1$, so $\boxed{a = 1 + \frac{1}{\sqrt{k}} \Rightarrow b = 1 + \sqrt{k}}$

Problem #6 (Elmore Delay, 10 points).

6-1. Compute Elmore delay at LOAD1 and LOAD2, i.e., represent the delay at LOAD1 (and LOAD2) as a function of $R_1 \sim R_4, C_1, C_2, C_{LOAD1}$, and C_{LOAD2}.



At LOAD1: $R_1(C_1 + C_2 + C_{LOAD1} + C_{LOAD2}) + R_2(C_2 + C_{LOAD1}) + R_3 C_{LOAD1}$

At LOAD2: $R_1(C_1 + C_2 + C_{LOAD1} + C_{LOAD2}) + R_4 C_{LOAD2}$

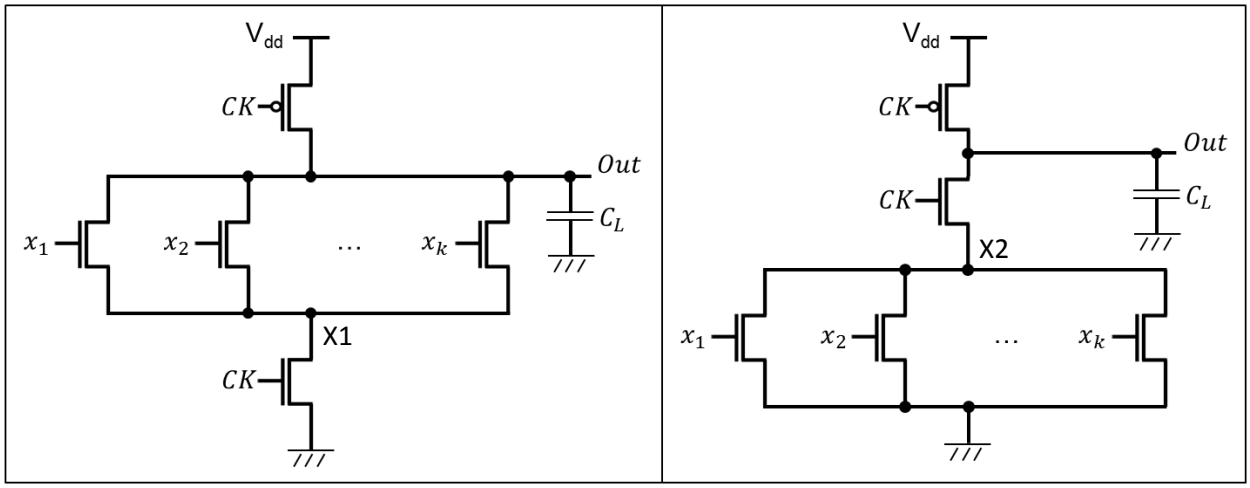
6-2. Compute Elmore delay at LOAD1 for $R_1 = R_2 = R_3 = 1k\Omega, C_1 = C_2 = C_{LOAD1} = 10fF, R_4 = \mathbf{0.1k\Omega}, and\ C_{LOAD2} = 1pF$. Then, compute Elmore delay at LOAD1 for $R_1 = R_2 = R_3 = 1k\Omega, C_1 = C_2 = C_{LOAD1} = 10fF, R_4 = \mathbf{10M\Omega}, and\ C_{LOAD2} = 1pF$. This result is called “resistive shielding”. Discuss a limitation of the Elmore delay model in terms of the resistive shielding effect.

At LOAD1: 1k(10f+10f+10f+1p) + 1k(10f+10f) + 1k(10f)=(1k*1030f) + (1k*20f) + (1k*10f) = 1030ps + 20ps + 10ps = 1060ps

The Elmore delay at LOAD1 is not affected by R_4. If R_4 is sufficiently small, the Elmore delay at LOAD1 should include C_{LOAD2}. However, if R_4 is sufficiently large, we can assume that the Load2 branch does not exist, so the Elmore delay at LOAD1 should not include C_{LOAD2}. The Elmore delay model does not distinguish these two cases.

Problem #7 (Dynamic CMOS, 10 points).

Compare the following implementations for a dynamic-CMOS *k*-input NOR gate. Are there any problems in (a)? in (b)?

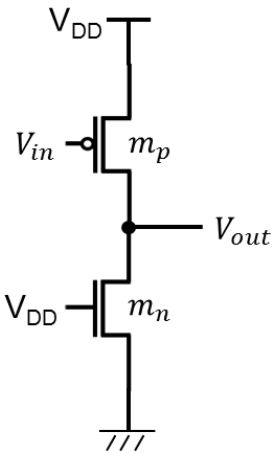


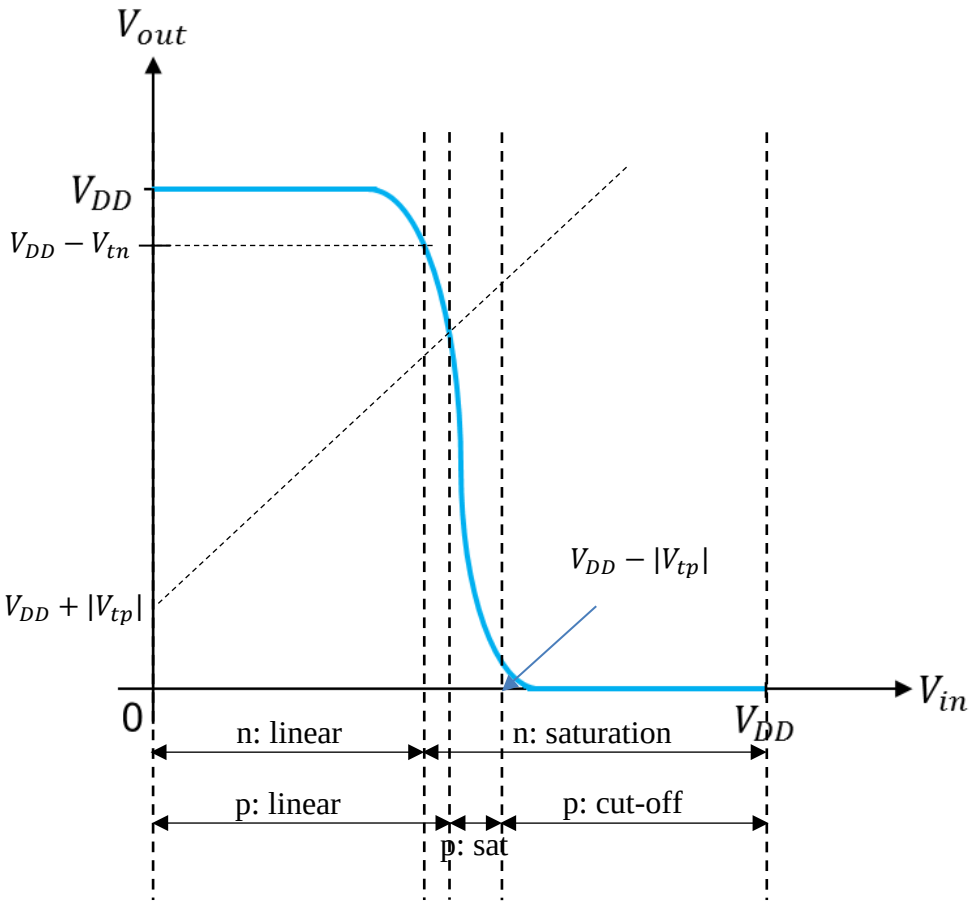
(a) does not have any charge sharing problem. When CK=0, the PMOS transistor charges the output capacitor and X1 (if any x_i is 1).

(b) suffers from charge sharing. When CK=1 and x_1=…=x_k=0, charge sharing happens between the output capacitor and the parasitic capacitor at X2.

Problem #8 (DC Characteristics, 10 points).

The following circuit is called “pseudo-PMOS”. Sketch a DC characteristic curve of the pseudo-PMOS inverter and properly split the curve into regions. In each region, show the status (cut-off, linear, saturation) of each transistor (m_n and m_p).





1) m_n: $V_{gs} - V_t = V_{DD} - V_{tn} > 0\ (always)\ , V_{ds} = V_{out}$

i) $V_{gs} - V_t < V_{ds}\ \Rightarrow\ V_{DD} - V_{tn} < V_{out}\ \Rightarrow saturation$

ii) $V_{DD} - V_{tn} > V_{out}\ \Rightarrow\ linear$

2) m_p: $|V_{gs}| - |V_t| = V_{DD} - V_{in} - |V_{tp}|\ , |V_{ds}| = V_{DD} - V_{out}$

i) $|V_{gs}| - |V_t| < 0\ \Rightarrow\ V_{in} > V_{DD} - |V_{tp}|\ \Rightarrow\ cut - off$

ii) $V_{gs} - V_t < V_{ds}\ \Rightarrow\ V_{out} < V_{in} + |V_{tp}| \Rightarrow\ saturation$

iii) $V_{gs} - V_t > V_{ds}\ \Rightarrow\ V_{out} > V_{in} + |V_{tp}| \Rightarrow\ linear$

*) Depending on the size of the NMOS and PMOS transistors, the highest output voltage might be less than $V_{DD} - V_{tn}$. In this case, the NMOS transistor is in the linear mode even when V_{in} is close to 0.