EE434

ASIC and Digital Systems

Final Exam

May 5, 2020. (8am – 10am)

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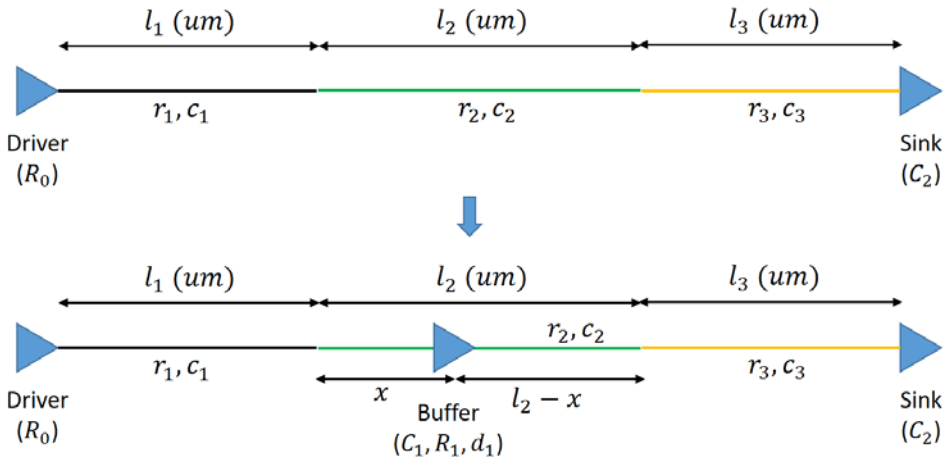
Name:

WSU ID:

Problem	Points	
1	30	
2	40	
3	30	
4	50	
5	20	
6	50	
7	40	
Total	260	

Problem #1 (Interconnects, 30 points)



The figure shows a net composed of three wire segments. The length and unit wire R and C of section k ($k = 1, 2, 3$) are l_k, r_k, and c_k, respectively as shown in the figure. The output resistance of the driver is R_0, the input capacitance of the sink is C_2, and the output resistance, input capacitance, and the delay of a buffer is R_1, C_1, and d_1, respectively. We are going to insert a buffer into the second section ($0 \le x \le l_2$). The first and third sections are not bufferable.

(a) Find the optimal location for the buffer insertion (express x as a function of the constants). (10 points)

(b) Answer the following questions. (Correct: +2 points. Wrong: -1 point. No answer: 0.)

(1) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x = \frac{1}{2} l_2$. (True / False)

(2) If $R_0 < R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / False)

(3) If $R_0 = R_1$, $C_1 < C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / False)

(4) If $R_0 = R_1$, $C_1 = C_2$, $r_1 < r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / False)

(5) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 > r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / False)

(6) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 < c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / False)

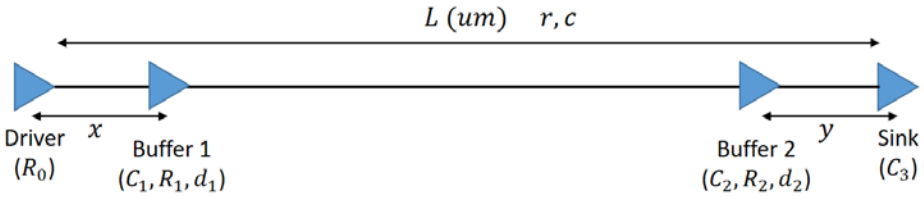
(7) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 > c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / False)

(8) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 < l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / False)

(9) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 > l_3$, then $x < \frac{1}{2} l_2$. (True / False)

(10) If r_3 increases, x increases (i.e., the optimal buffer location is shifted to the right.) (True / False)

Problem #2 (Interconnects, 40 points)



The figure shows a net composed of a long wire whose unit resistance and capacitance are r and c, respectively. We want to insert two buffers, Buffer 1 and Buffer 2 ($0 \le x$, $0 \le y$, $x + y \le L$). The output resistance ($R_{\#}$), input capacitance ($C_{\#}$), and internal delay ($d_{\#}$) of each cell are shown above.

(a) Find the optimal locations for Buffer 1 and Buffer 2 (express x (and also y) as a function of the constants). Hint: Express the total delay as a function of x and y. Then, different it w.r.t. x and set it to zero. Differentiate it w.r.t. y and set it to zero. Then, you get two equations for two variables, x and y. Solve it. (12 points)

$x =$

$y =$

(b) Answer the following questions. (Correct: +2 points. Wrong: -1 point. No answer: 0.)

Notice that if x increases, Buffer 1 is shifted to the right.

However, if y increases, Buffer 2 is shifted to the left.

(1) If $R_0 = R_1 = R_2$ and $C_1 = C_2 = C_3$, then $x = \frac{1}{3}L$. (True / False)

(2) If $R_0 = R_1 = R_2$ and $C_1 = C_2 = C_3$, then $y = \frac{1}{3}L$. (True / False)

(3) If R_0 increases, x increases. (True / False)

(4) If R_0 increases, y increases. (True / False)

(5) If R_1 increases, x increases. (True / False)

(6) If R_1 increases, y increases. (True / False)

(7) If R_2 increases, x increases. (True / False)

(8) If R_2 increases, y increases. (True / False)

(9) If C_1 increases, x increases. (True / False)

(10) If C_1 increases, y increases. (True / False)

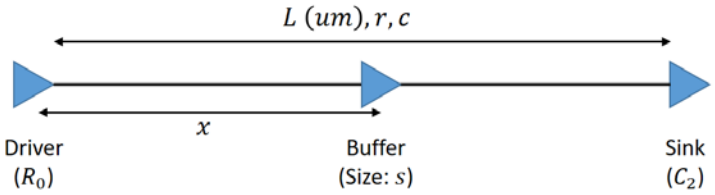
(11) If C_2 increases, x increases. (True / False)

(12) If C_2 increases, y increases. (True / False)

(13) If C_3 increases, x increases. (True / False)

(14) If C_3 increases, y increases. (True / False)

Problem #3 (Interconnects, 30 points)



The figure shows a long wire whose length, unit resistance and capacitance are L, r, and c, respectively. We want to insert a buffer ($0 \leq x \leq L$). The size of the buffer is s and its output resistance, input capacitance, and internal delay are as follows:

- Output resistance: $\frac{R}{s}$ (where R is a constant)
- Input capacitance: sP (where P is a constant)
- Internal delay: sD (where D is a constant)

Notice that there are two variables, x and s.

(a) Express the total delay as a function of the variables and the constants. (7 points)

$\tau =$

(b) Assuming the location (x) is given (i.e., you can treat it as a constant.), find the optimal size (s) of the buffer, .i.e., express the optimal value of s as a function of the constants and x. (7 points)

$s =$

(c) Answer the following questions. (Correct: +2 points. Wrong: -1 point. No answer: 0.)

(1) If x increases, s increases. (True / False)

(2) If R increases, s increases. (True / False)

(3) If c increases, s increases. (True / False)

(4) If C_2 increases, s increases. (True / False)

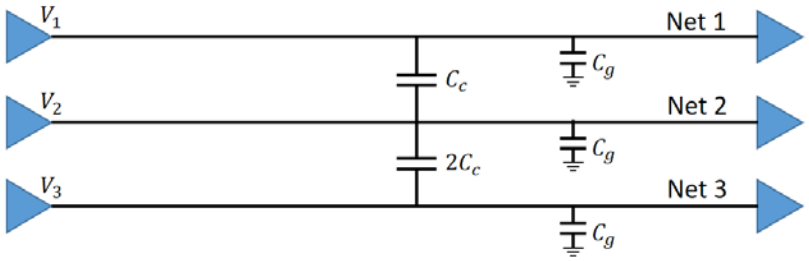
(5) If R_0 increases, s increases. (True / False)

(6) If r increases, s increases. (True / False)

(7) If P increases, s increases. (True / False)

(8) If D increases, s increases. (True / False)

Problem #4 (Coupling, 50 points)



The figure shows three parallel nets. The coupling capacitance between Net 1 and Net 2 is C_C. The coupling capacitance between Net 2 and Net 3 is $2C_C$. The following shows a three-bit binary encoding technique for four decimal numbers (0, 1, 2, 3).

Value	Encoding
0	000
1	010
2	101
3	111

(1) Calculate the total effective capacitance of Net 1 for all possible transitions (0→1, 0→2, 0→3, 1→0, 1→2, 1→3, 2→0, 2→1, 2→3, 3→0, 3→1, 3→2) for the encoding technique, i.e., calculate the sum of the effective capacitances of Net 1 for all possible transitions. (10 points)

(2) Repeat it for Net 2. (10 points)

(3) Repeat it for Net 3. (10 points)

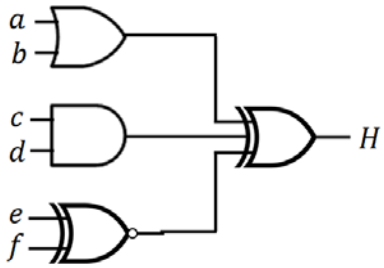
(4) Find a new three-bit encoding of the four values (0, 1, 2, 3) that minimizes the total effective capacitance of the three nets for all possible transitions (Assume $C_g = C_c$). (20 points)

Value	Encoding
0	
1	
2	
3	

Total effective capacitance (for Net 1 + for Net 2 + for Net 3):

Problem #5 (Testing, 20 points)

The following shows $H = (a + b) \oplus (c \cdot d) \oplus (\overline{e \oplus f})$. Answer the following questions.

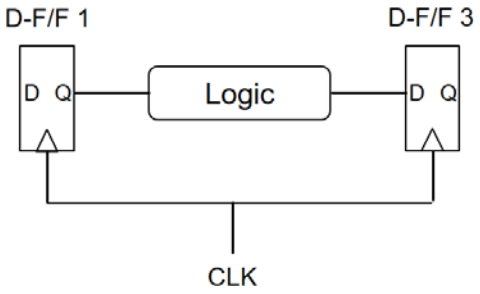


(1) Find all input vectors that can detect a s-a-0 fault at input a. (10 points)

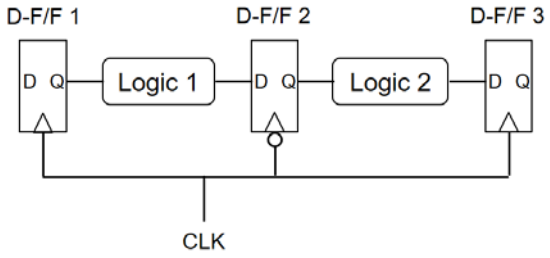
(2) Find all input vectors that can detect a s-a-1 fault at input e. (10 points)

Problem #6 (Static Timing Analysis, 50 points)

The following shows two pipelining methodologies. Figure (a) shows a logic in a single pipeline stage. Figure (b) shows a partitioned version in which two pipeline stages are cascaded and the flip-flop in the middle is negative-edge-triggered.



(a)



(b)

Parameters

- d_1, d_2, d_3: The delay from the clock source to Flip-Flop 1, 2, 3
- c_1, c_2, c_3: Clock-to-Q delay (T_{CQ}) of Flip-Flop 1, 2, 3
- s_1, s_2, s_3: Setup time of Flip-Flop 1, 2, 3
- T_A, T_B : Clock period for Figure (a) and (b)
- N ($\gg 1$): # instructions to execute
- T_L: The logic delay in Figure (a). In Figure (b), the delay of each logic is $\frac{T_L}{2}$.
- Execution time of the system in Figure (a): $(N+1) \cdot T_A$
- Execution time of the system in Figure (b): $(N+3) \cdot T_B$

For the clock periods, we use the minimum clock periods that satisfy all the setup time constraints. Notice that the clock duty cycle is 50%.

(1) The system in Figure (a) has one setup time constraint. Show the inequality. (10 points)

Answer: $\leq T_A$

(2) The system in Figure (b) has two setup time constraints. Show the inequalities. (16 points)

Answer: $\leq \frac{T_B}{2}$

$\leq \frac{T_B}{2}$

You can merge these two inequalities by just adding them.

$$\leq T_B$$

Use the left term for the next problems.

(3) Now, you have execution times for Figure (a) and (b). Answer the following questions. (24 points)

(a) For Figure (a): If d_1 increases, the execution time increases (True / False).

(b) For Figure (a): If c_1 increases, the execution time increases (True / False).

(c) For Figure (a): If T_L increases, the execution time increases (True / False).

(d) For Figure (a): If d_3 increases, the execution time increases (True / False).

(e) For Figure (a): If s_3 increases, the execution time increases (True / False).

(f) For Figure (b): If d_1 increases, the execution time increases (True / False).

(g) For Figure (b): If c_1 increases, the execution time increases (True / False).

(h) For Figure (b): If T_L increases, the execution time increases (True / False).

(i) For Figure (b): If d_3 increases, the execution time increases (True / False).

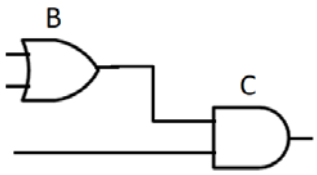
(j) For Figure (b): If s_2 increases, the execution time increases (True / False).

(k) For Figure (b): If s_3 increases, the execution time increases (True / False).

(l) For Figure (b): If c_2 increases, the execution time increases (True / False).

Problem #7 (Static Timing Analysis, 40 points)

The following shows two gates B and C, which are in the middle of a circuit.



“A gate has a (setup or hold) time violation” means that at least one of the paths going through the gate violates given (setup or hold) time constraints.

(1) Is it possible that gate B has a setup-time violation and gate C has a setup-time violation? Explain why.

(2) Is it possible that gate B has a setup-time violation and gate C has a hold-time violation? Explain why.

(3) Is it possible that gate B has a hold-time violation and gate C has a setup-time violation? Explain why.

(4) Is it possible that gate B has a hold-time violation and gate C has a hold-time violation? Explain why.