EE466

VLSI System Design

Midterm Exam

Oct. 25, 2018. (4:15pm – 5:30pm)

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Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	5	
4	10	
5	5	
6	10	
7	10	
8	10	
Total	70	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

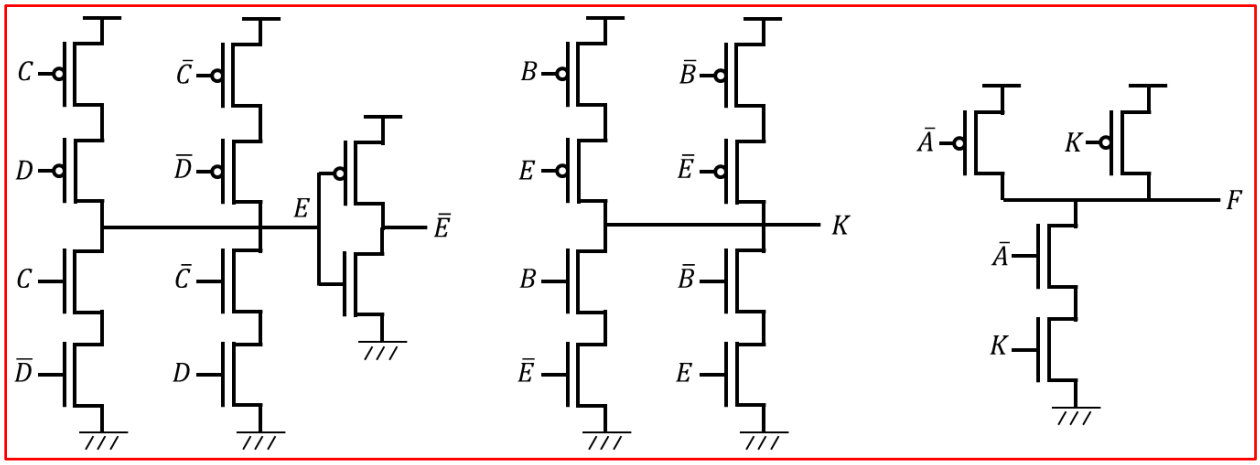
Problem #1 (Static CMOS Gates, 10 points).

Draw a transistor-level schematic for the following Boolean function (Available input: $A, B, C, D, \bar{A}, \bar{B}, \bar{C}, \bar{D}$). Use the static CMOS gate design. Minimize the # TRs.

TRs≤ 22: 10 points. 23≤# TRs≤24: 8 points. 25≤# TRs≤26: 6 points. 27≤# TRs: 4 points.

$$F = A + \left(B \oplus \left(\overline{C \oplus D}\right)\right)$$

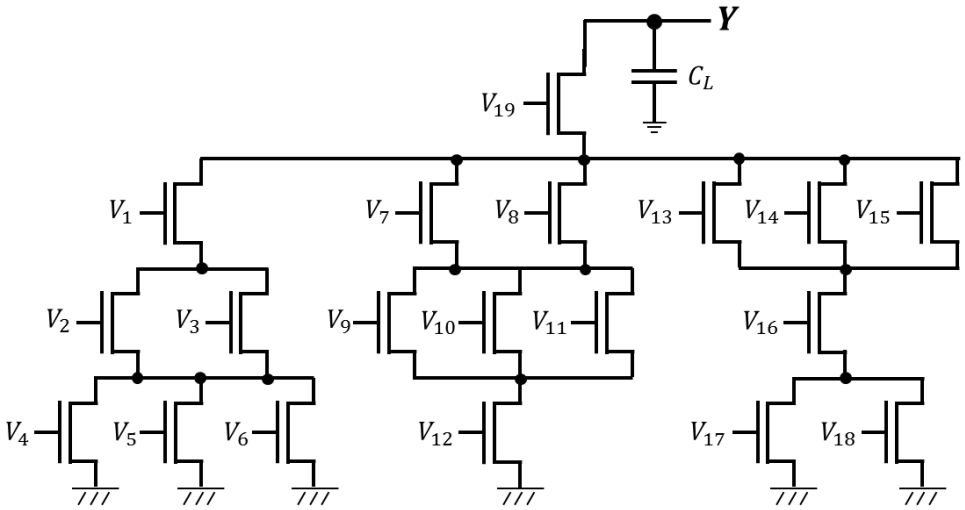
$$F = \overline{\overline{A + \left(B \oplus \left(\overline{C \oplus D}\right)\right)}} = \overline{\bar{A} \cdot \overline{B \oplus \left(\overline{C \oplus D}\right)}}$$



Problem #2 (Transistor Sizing, 10 points).

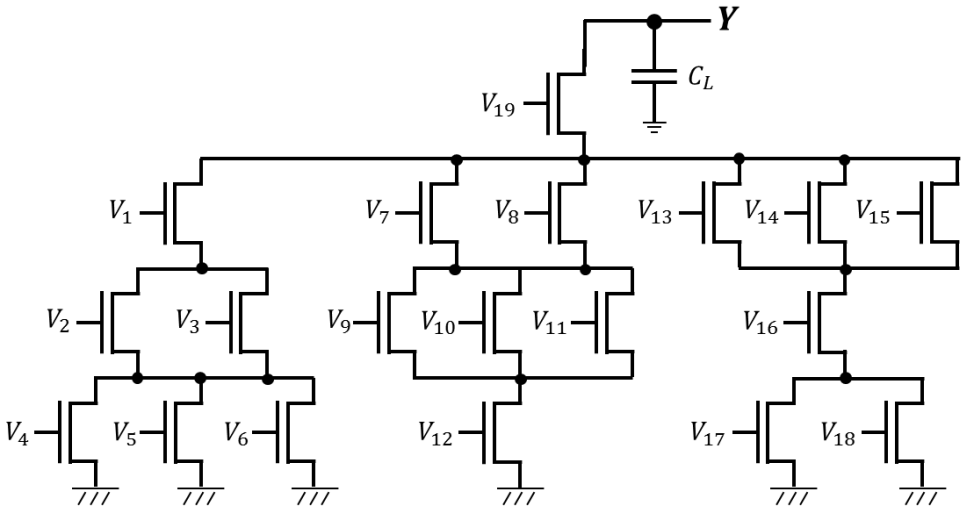
Size the transistors in the following pull-down network of a static CMOS gate. R_n is the resistance of a 1X NMOS transistor. C_L is the load cap. Ignore parasitic capacitances. Target timing constraint: $\tau = R_n \cdot C_L$. Try to minimize the total area.

Area≤80X: 10 points. 80X<Area≤82X: 8 points. 82X<Area≤84X: 6 points. 84X<Area: 4 points.



The worst case is that only one path is activated (e.g., V_{19}, V_1, V_2, V_4). Thus, each of them is upsized to 4X. Thus, all of them are upsized to 4X. Total area: 76X.

Problem #3 (Switching Analysis, 5 points).



All the transistors in the figure shown above have the same width W. Ignore parasitic RC. All the inputs are 0V at time 0. At time t, some of the input voltages switch from 0 to V_{DD}. Which one of the following has the smallest falling delay?

1) V_{19}, V_1, V_2, V_5 switch from 0 to VDD. $R = \frac{4}{w}$

2) $V_{19}, V_1, V_2, V_3, V_5$ switch from 0 to VDD. $R = \frac{1}{w} + \frac{1}{2w} + \frac{1}{w} + \frac{1}{w} = \frac{7}{2w} = \frac{3.5}{w}$

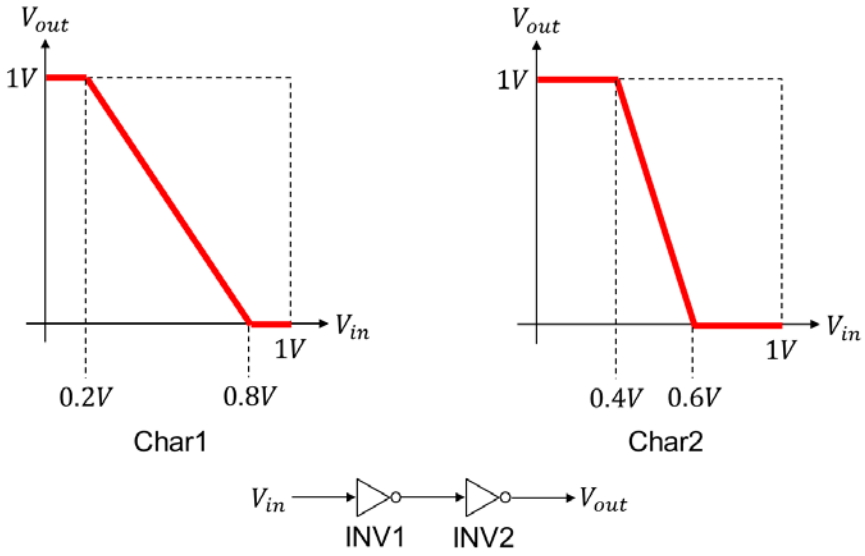
3) $V_{19}, V_7, V_8, V_{10}, V_{12}$ switch from 0 to VDD. $R = \frac{3.5}{w}$

4) $V_{19}, V_7, V_9, V_{12}, V_{13}, V_{14}, V_{15}, V_{16}$ switch from 0 to VDD. $R = \frac{4}{w}$

5) $V_{19}, V_1, V_2, V_6, V_7, V_9, V_{12}, V_{13}, V_{16}, V_{18}$ switch from 0 to VDD. $R = \frac{3}{3w} + \frac{1}{w} = \frac{2}{w}$

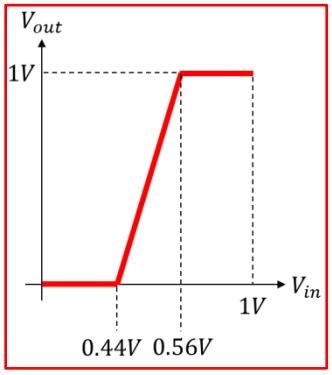
6) $V_{19}, V_1, V_2, V_4, V_7, V_8, V_9, V_{10}, V_{11}, V_{13}, V_{14}, V_{15}, V_{16}$ switch from 0 to VDD. $R = \frac{4}{w}$

Problem #4 (DC Analysis, 10 points).

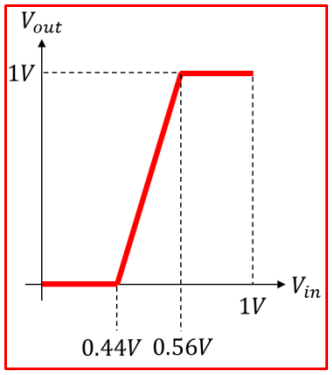


The gate-level schematic shows a buffer composed of two inverters.

1) Draw a DC characteristic curve (Char1 is for INV1 and Char2 is for INV2). You should show not only the curve, but also some important numbers in the curve.

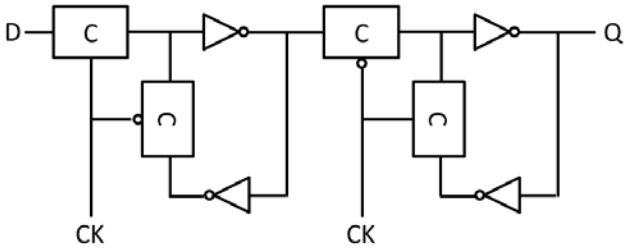


2) Draw a DC characteristic curve (Char1 is for INV2 and Char2 is for INV1). You should show not only the curve, but also some important numbers in the curve.

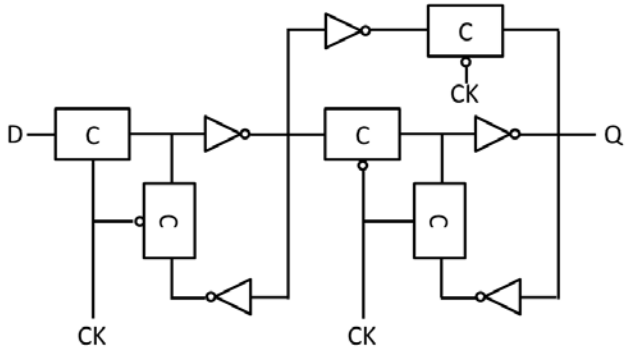


Problem #5 (Sequential Logic, 5 points).

The following shows a schematic of a positive-edge-triggered D-FF.

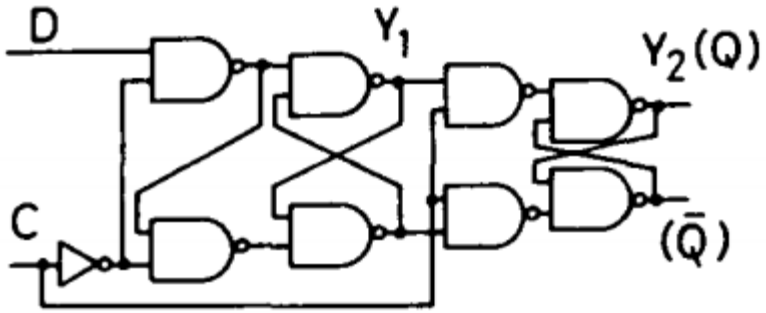


What does the following circuit do? Can you explain any differences between the two circuits?



The second one is also a positive-edge-triggered D-FF. The Clock-to-Q delay of the second one is shorter than that of the first one.

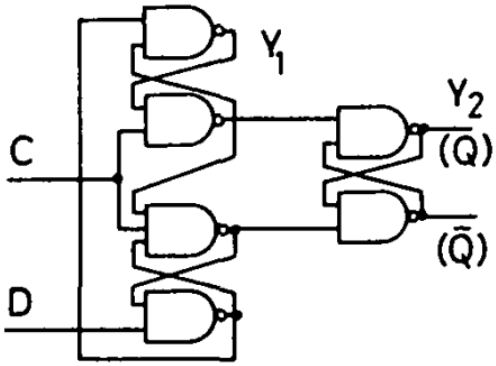
Problem #6 (Sequential Logic, 10 points).



Describe the function of the circuit shown above.

It is a positive-edge-triggered D-FF.

Problem #7 (Sequential Logic, 10 points).



Describe the function of the circuit shown above.

It is a positive-edge-triggered D-FF.

Problem #8 (Static CMOS Gates, 10 points).

Draw a dual PFET network of the following NFET network between nodes X and Y. Use eight PFETs only.