

EE466

VLSI System Design

Midterm Exam

Oct. 24, 2018. (4:15pm – 5:30pm)

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Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
Total	80	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Static CMOS Gates, 10 points).

Draw a transistor-level schematic for the NFET network of the following Boolean function (Available input: $A, B, C, D, \bar{A}, \bar{B}, \bar{C}, \bar{D}$). Use the static CMOS gate design. Minimize the # TRs.

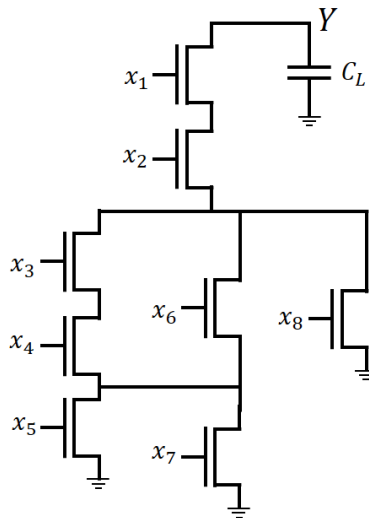
TRs \leq 12: 10 points. 13 \leq # TRs \leq 14: 8 points. 15 \leq # TRs \leq 16: 5 points.

$$F = \overline{A \oplus (B \oplus (CD))}$$

Problem #2 (Transistor Sizing, 10 points).

Size the transistors in the following pull-down network of a static CMOS gate. R_n is the resistance of a 1X NMOS transistor. C_L is the load cap. Ignore all the parasitic capacitances. Target timing constraint: $\tau = R_n \cdot C_L$. Try to minimize the total area.

Area $\leq 36X$: 10 points. $36X < \text{Area} \leq 38X$: 7 points. $38X < \text{Area}$: 4 points.



x_1 :

x_2 :

x_3 :

x_4 :

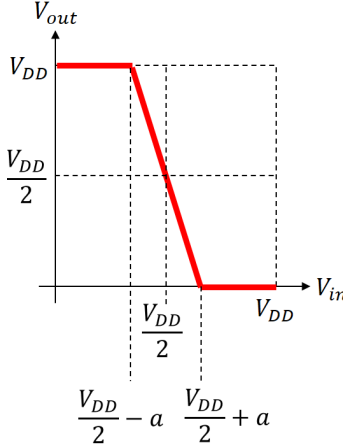
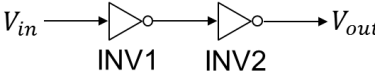
x_5 :

x_6 :

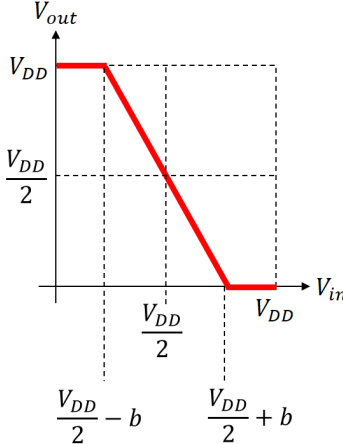
x_7 :

x_8 :

Problem #3 (DC Analysis, 10 points).



Char 1



Char 2

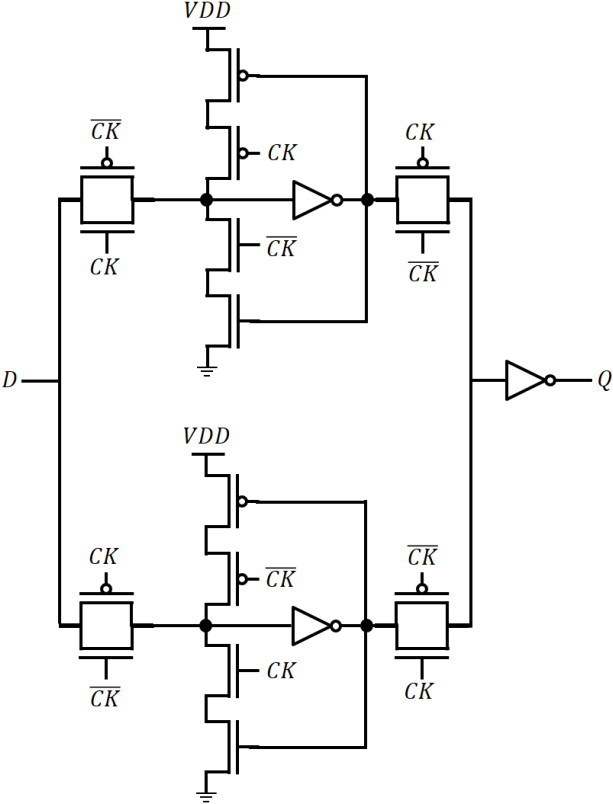
The gate-level schematic shows a buffer composed of two inverters.

Buffer 1: Char 1 for INV1 and Char 2 for INV2

Buffer 2: Char 2 for INV1 and Char1 for INV2

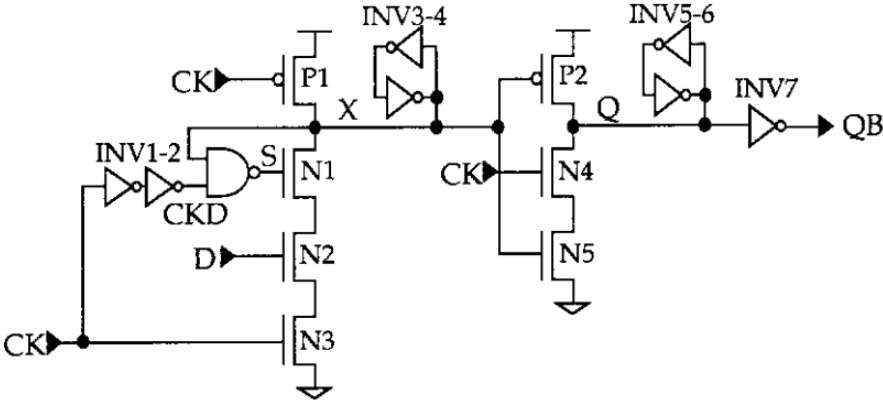
Prove that the two buffers have the same DC characteristics.

Problem #4 (Logic Analysis, 10 points).



Describe the function of the circuit shown above.

Problem #5 (Sequential Logic, 10 points).

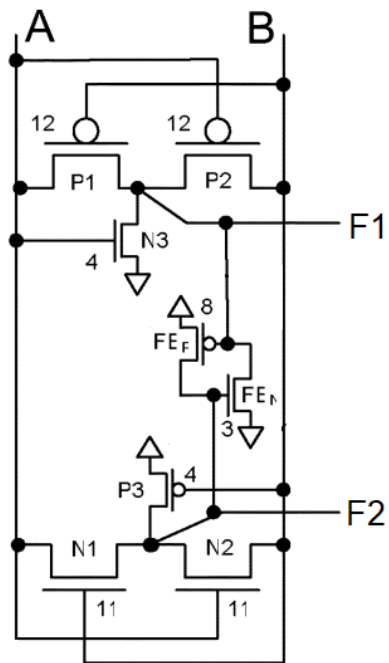


The circuit shown above is a positive-edge-triggered D FF.

(1) Estimate the hold time of the FF for input D=0.

(2) Estimate the hold time for input D=1.

Problem #6 (Logic Analysis, 10 points).



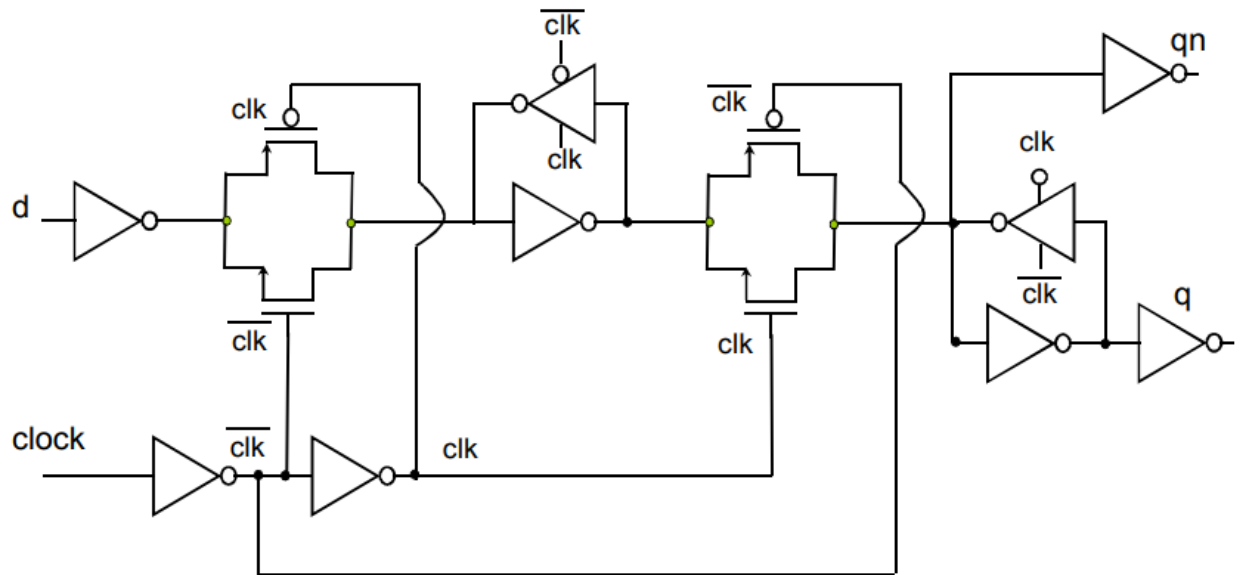
The above circuit has two inputs (A, B) and two outputs (F1 and F2).

(1) Express F1 as a Boolean function of A and B.

(2) Express F2 as a Boolean function of A and B.

(3) Does it have any static power consumption problem? Explain why (or why not).

Problem #7 (Sequential Logic, 10 points).



The circuit shown above is a positive-edge-triggered D FF. Notice that all the inverters and transmission gates have finite delays.

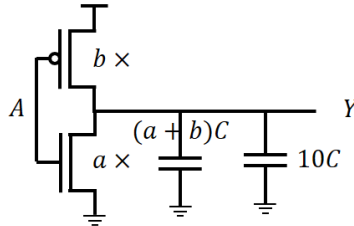
(1) Estimate the hold time of the FF for input $D=0$.

(2) Estimate the hold time for input $D=1$.

(3) Estimate the signal delay (from a clock rising edge at the clock input to Q).

Problem #8 (Power Consumption, 10 points).

The following figure shows an inverter with a parasitic cap and a load cap ($10C$). The parasitic cap is proportional to the sizes of the transistors connected to the cap. The PFET is upsized to bX and the NFET is upsized to aX . $\frac{\mu_n}{\mu_p} = 2$. The rising delay should be $\leq 20R_nC$ where R_n is the resistance of a $1X$ NFET. The falling delay should be $\leq 10R_nC$. Both a and b are integers.



Can you find a and b minimizing the power consumption and satisfying the given timing constraints? Notice that there are only a few combinations of (a, b) you need to calculate to answer this problem.