EE434

ASIC and Digital Systems

Final Exam

May 5, 2016. (1pm – 3pm)

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Name:

WSU ID:

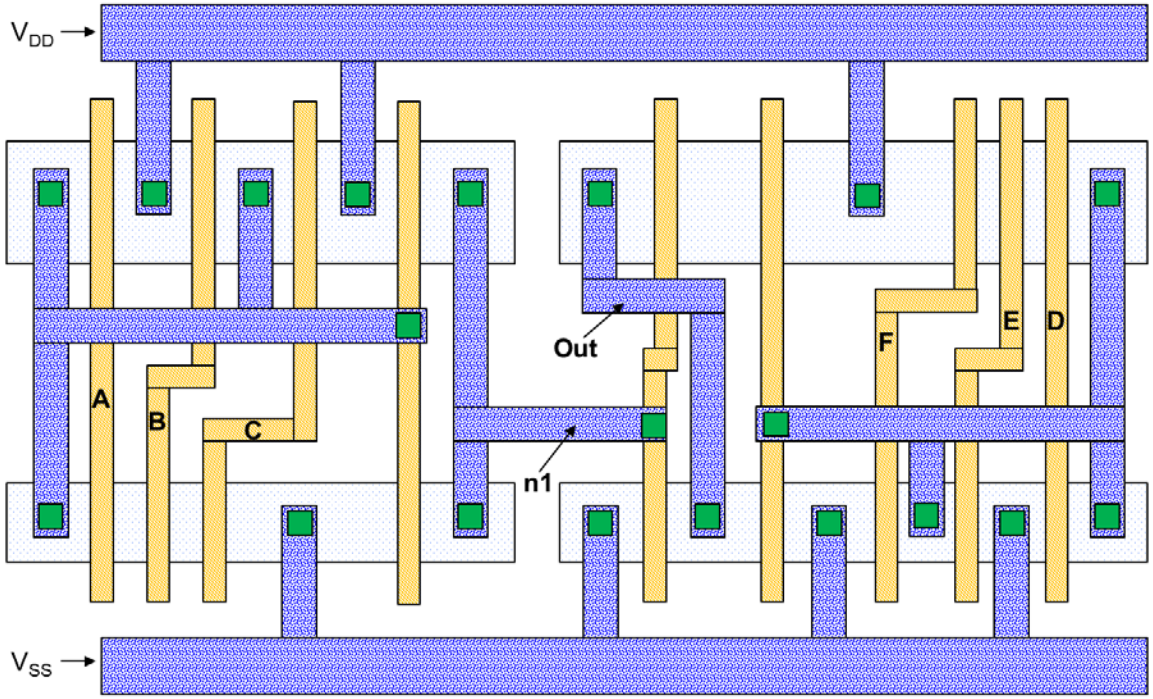
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
Total	80	

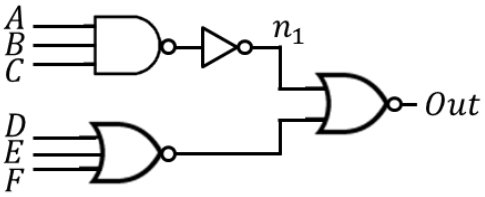
* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Layout + Testing, 10 points)

The following layout consists of six primary inputs (A, B, C, D, E, F) and a primary output (Out). n1 is an internal node. Find all input vectors that can detect a stuck-at-0 fault at node n1.





$$Out = \overline{\overline{ABC} + \overline{D + E + F}} = \overline{ABC} \cdot (D + E + F)$$

$$Out_f = D + E + F$$

$$Out \oplus Out_f = 1 \rightarrow \ ABC = 1, D + E + F = 1$$

$$\rightarrow ABCDEF = 111001, 111010, 111011, 111100, 111101, 111110, 111111$$

Problem #2 (Testing, 10 points)

A combinational logic has n inputs ($x_1, x_2, \dots, x_n$) and an output (Z). Z is a Boolean function of the inputs, $Z = g(x_1, \dots, x_n, \overline{x_1}, \dots, \overline{x_n}, AND, OR)$. To find input vectors that can detect a stuck-at-v fault f at a node, we compute Z_f by setting the value of the node to v and solving $Z \oplus Z_f = 1$. Let T_1 be a set of all input vectors that detect fault f_1 and T_2 be a set of all input vectors that detect fault f_2 ($f_1 \neq f_2$). Prove that if $Z_{f1} \neq Z_{f2}$, T_1 cannot be equal to T_2.

(Example: A three-input AND gate has three inputs a, b, c and an output Z. Let f_1 be a stuck-at-0 fault at input a and f_2 be a stuck-at-1 fault at input b. Then, $Z = a \cdot b \cdot c, Z_{f1} = 0, Z_{f2} = a \cdot c$ ($Z_{f1} \neq Z_{f2}$). In this case, $T_1 = \{111\}$ and $T_2 = \{101\}$, so $T_1 \neq T_2$.)

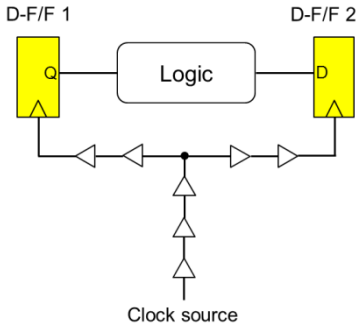
First, we prove that if $Z_{f1} = Z_{f2}$, $T_1 = T_2$.

We get T_1 from $Z \oplus Z_{f1} = 1$ and T_2 from $Z \oplus Z_{f2} = 1$. Thus, if $Z_{f1} = Z_{f2}$, $T_1 = T_2$.

Now, suppose there exists a case where $T_1 = T_2$ when $Z_{f1} \neq Z_{f2}$ (i.e., if $Z_{f1} \neq Z_{f2}$, then $T_1 = T_2$). The contrapositive of this statement is "If $T_1 \neq T_2$, then $Z_{f1} = Z_{f2}$". However, this is a contradiction because if $Z_{f1} = Z_{f2}$, then $T_1 = T_2$ by the proof shown above. Thus, the original statement "if $Z_{f1} \neq Z_{f2}$, then $T_1 = T_2$" is also false, i.e., if $Z_{f1} \neq Z_{f2}$, T_1 cannot be equal to T_2.

Problem #3 (Timing Analysis, 10 points).

- Setup time of the F/Fs: T_{s}
- Hold time of the F/Fs: T_{h}
- D-F/F internal delay: T_{CQ}
- Clock skew: T_{skew} = delay from the clock source to D-FF2 – delay from the clock source to D-FF1
- Logic delay: T_{logic}
- Clock period: T_{CLK}
- Buffer delay: T_{b}

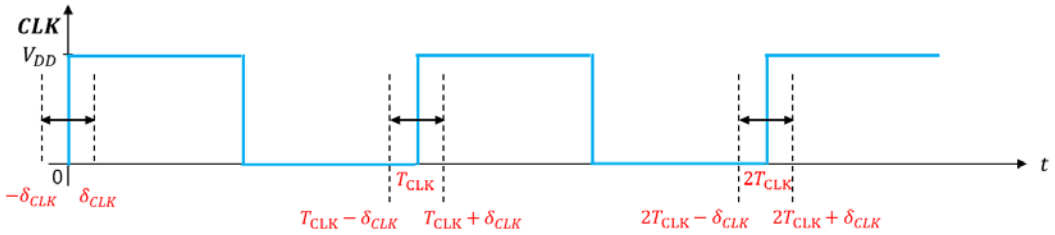


There are five buffers between the clock source and the clock pin of D-FF1 (and D-FF2) as shown in the figure. Ideally, the following inequalities should be satisfied:

- Setup time: $T_{\mathrm{s}} \leq T_{\mathrm{CLK}} + T_{\mathrm{skew}} - T_{\mathrm{logic}} - T_{\mathrm{CQ}}$
- Hold time: $T_{\mathrm{h}} \leq T_{\mathrm{CQ}} + T_{\mathrm{logic}} - T_{\mathrm{skew}}$

However, there exist uncertainties such as delay variations due to temperature, so we should incorporate those uncertainties (variations) into the setup and hold time inequalities. The followings show the variation sources we are going to consider:

- $T_{\mathrm{b}} \rightarrow T_{\mathrm{b}} \pm \delta_b$
- $T_{\mathrm{CQ}} \rightarrow T_{\mathrm{CQ}} \pm \delta_{CQ}$
- $T_{\mathrm{logic}} \rightarrow T_{\mathrm{logic}} \pm \delta_{logic}$
- Clock jitter: $\pm\delta_{CLK}$



<u>Derive a new setup time and a new hold time constraints (inequalities) that should be satisfied under the variations.</u>

Setup time constraint:

Suppose the first clock leaves the clock source at time 0 and the second clock leaves at time T_{CLK} ideally. Then, the minimum arrival time of the second clock at DFF2 is $T_{CLK} - \delta_{CLK} + 5T_b - 5\delta_b$ and the maximum arrival time of the first clock at DFF1 is $\delta_{CLK} + 5T_b + 5\delta_b$, so the minimum skew is $-2\delta_{CLK} - 10\delta_b$. The maximum logic+CQ delay is $T_{logic} + \delta_{logic} + T_{CQ} + \delta_{CQ}$. Thus, the new setup time constraint is

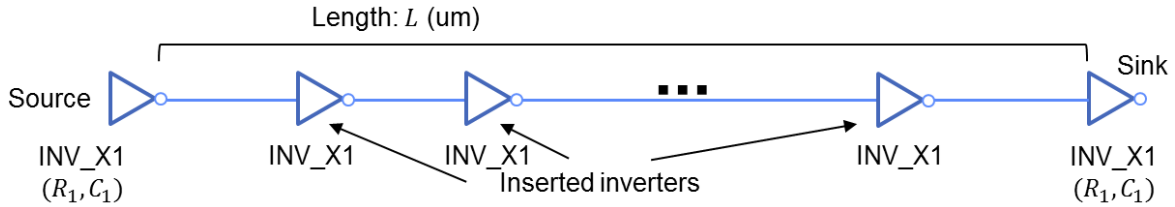
$$T_s \leq T_{CLK} - 2\delta_{CLK} - 10\delta_b - (T_{logic} + \delta_{logic} + T_{CQ} + \delta_{CQ})$$

Hold time constraint:

The minimum arrival time of the first clock at DFF1 is $-\delta_{CLK} + 5T_b - 5\delta_b$ and the maximum arrival time of the first clock at DFF2 is $\delta_{CLK} + 5T_b + 5\delta_b$, so the maximum skew is $2\delta_{CLK} + 10\delta_b$. The minimum logic+CQ delay is $T_{logic} + \delta_{logic} - T_{CQ} - \delta_{CQ}$. Thus, the new hold time constraint is

$$T_h \leq \left(T_{logic} - \delta_{logic} + T_{CQ} - \delta_{CQ}\right) - (2\delta_{CLK} + 10\delta_b)$$

Problem #4 (Interconnect Optimization, 10 points)



A buffer is composed of two inverters, so it consumes more power than an inverter. Thus, we can insert inverters instead of buffers to optimize a net while minimizing power consumption. However, only an even number of inverters can be inserted (if the inverter count is odd, there will be signal inversion).

In the above figure, the driver, the sink, and the inserted inverters have the same input capacitance (C_1) and output resistance (R_1), so the inserted inverters should be evenly distributed between the source and the sink. Now, suppose the optimal number of inverters we find is k where k is odd. Since k is odd, we have to insert either $k-1$ or $k+1$ inverters. Which will lead to a better result (shorter delay)? $k-1$ or $k+1$? Show all the details about your answer.

- Net length: L (um)
- Inverter output resistance and input capacitance: R_1, C_1
- Unit wire resistance and capacitance: r, c
- Inverter delay: d

Suppose we insert $p-1$ inverters and evenly distribute them. Then, the delay will be

$$\tau(p-1) = p \cdot \left\{ R_1 \left(\frac{cL}{p} + C_1 \right) + \frac{rL}{p} C_1 + 0.5rc \left(\frac{L}{p} \right)^2 \right\} + (p-1) \cdot d$$

$$= R_1 cL + rLC_1 - d + pR_1 C_1 + pd + \frac{0.5rcL^2}{p} = \alpha + p(R_1 C_1 + d) + \frac{0.5rcL^2}{p}$$

(α is a constant)

If we insert $k-1$ inverters, the delay becomes

$$\tau(k-1) = \alpha + k(R_1 C_1 + d) + \frac{0.5rcL^2}{k}$$

and if we insert $k+1$ inverters, the delay becomes

$$\tau(k+1) = \alpha + (k+2)(R_1 C_1 + d) + \frac{0.5rcL^2}{k+2}$$

Thus, $\Delta = \tau(k+1) - \tau(k-1) = 2(R_1C_1 + d) + 0.5rcL^2\left(\frac{1}{k+2} - \frac{1}{k}\right)$

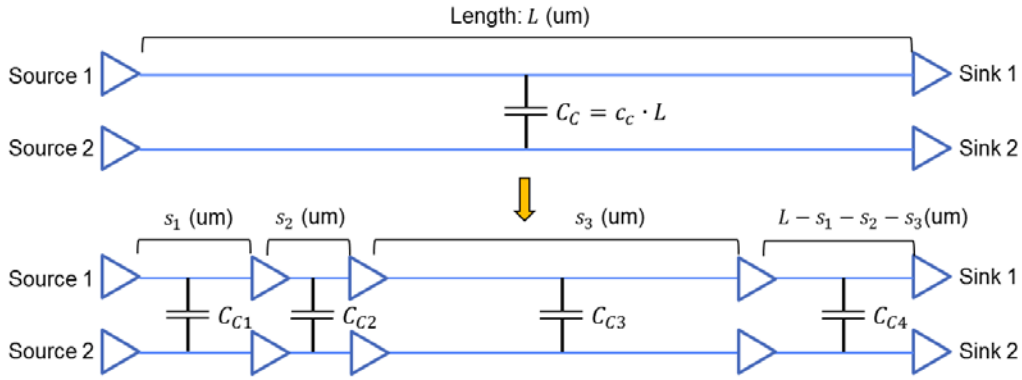
$$= 2(R_1C_1 + d) - \frac{2rcL^2}{k^2 + 2k}$$

$\Delta > 0 \rightarrow \quad k > -1 + \sqrt{1 + \frac{rcL^2}{(R_1C_1 + d)}}$

Thus, if $k > -1 + \sqrt{1 + \frac{rcL^2}{(R_1C_1 + d)}}$, inserting $k - 1$ inverters is better.

If $k < -1 + \sqrt{1 + \frac{rcL^2}{(R_1C_1 + d)}}$, inserting $k + 1$ inverters is better.

Problem #5 (Interconnect Optimization, 10 points).



Two nets are routed as shown above. The coupling capacitance between them is C_c. You are supposed to insert buffers into the nets identically as shown above. All the drivers, sinks, and buffers are of the same type. The following list shows all the parameters and variables you should use:

- Output resistance: R
- Input capacitance: C
- Total length: L (um)
- Unit wire resistance: r_w/um
- Unit wire capacitance: c_w/um
- Unit coupling capacitance: c_c/um
- Buffer delay: d

Insert buffers into the nets optimally, i.e., find the number of buffers to insert and their locations to minimize the delay of the nets.

In the worst case (i.e., the signal pattern of Source 1 is 0101… and that of Source 2 is 1010…), the total capacitance of a segment whose length is $k(um)$ is $k(c_w + 2c_c)$. Suppose we insert $p - 1$ buffers and the length of the m-th segment is s_m. Then, the total delay is

$$\tau = (p-1)\cdot d + \sum_{i=1}^{p}[R\cdot\{s_i\cdot(c_w+2c_c)+C\} + s_i\cdot r_w\cdot C + 0.5r_w(c_w+2c_c)s_i{}^2]$$

$$= (p-1)\cdot d + R\cdot(c_w+2c_c)\cdot L + pRC + r_w\cdot L\cdot C + 0.5r_w(c_w+2c_c)\cdot\left(s_1{}^2+\cdots+s_p{}^2\right)$$

$$\frac{\partial\tau}{\partial s_i} = 0.5r_w(c_w+2c_c)\{2s_i - 2s_p\} = 0 \rightarrow \; s_1 = s_2 = \cdots = s_p$$

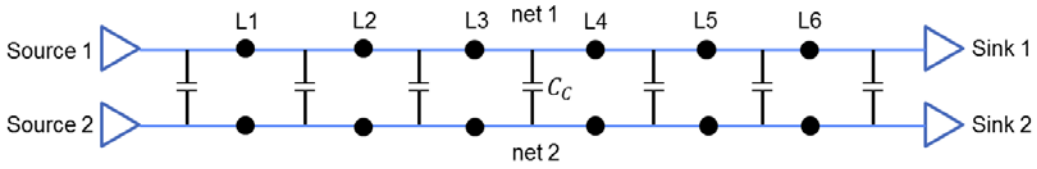
$$\therefore \tau = (p-1)\cdot d + R\cdot(c_w + 2c_c)\cdot L + pRC + r_w \cdot L \cdot C + 0.5 r_w (c_w + 2c_c)\cdot \frac{L^2}{p}$$

$$\frac{d\tau}{dp} = d + RC - \frac{r_w(c_w + 2c_c)L^2}{2p^2} = 0 \rightarrow \quad p = \sqrt{\frac{r_w(c_w + 2c_c)L^2}{2(RC + d)}}$$

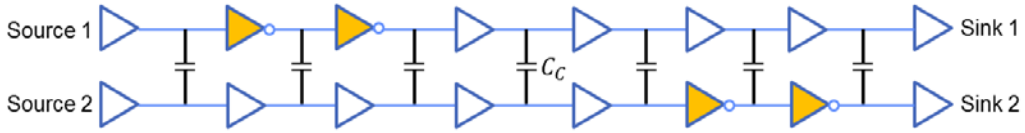
$$\therefore \#\, buffers = \sqrt{\frac{r_w(c_w + 2c_c)L^2}{2(RC + d)}} - 1$$

(and we evenly distribute the buffers).

Problem #6 (Interconnect Optimization, 10 points).



Two nets (net 1 and net 2) are coupled as shown above and you are supposed to insert a repeater (inverter or buffer) into each of the designated locations (L1 ~ L6). For instance, the following figure shows a repeater insertion solution (its delay and area are $12d$ and $20S$, respectively):



The following list shows the parameters used in this problem:

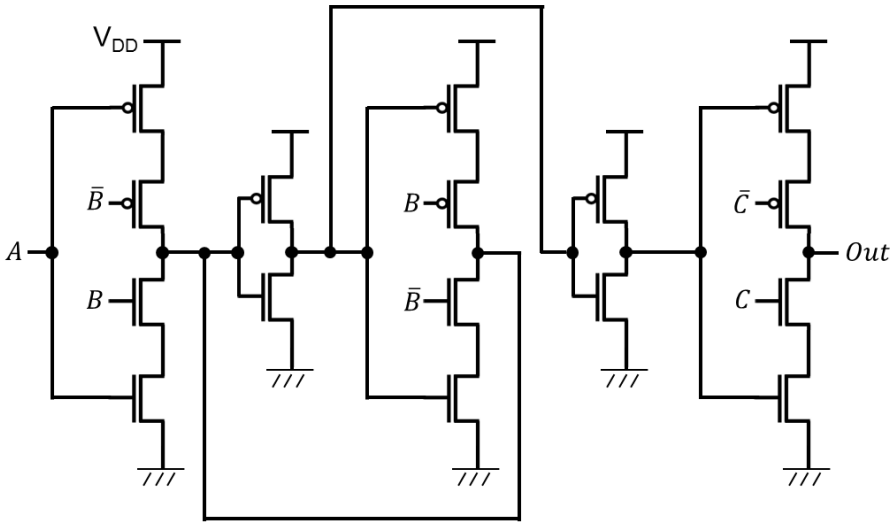
- Area of an inverter: S
- Area of a buffer: $2S$
- Delay of a net segment whose total capacitance is C_g: d
- Delay of a net segment whose total capacitance is $C_g + C_c$: $1.5d$
- Delay of a net segment whose total capacitance is $C_g + 2C_c$: $2d$
- Input pattern of net 1: 010101…
- Input pattern of net 2: 101010…
- Signal inversion at the sinks is not allowed.

The goal is to optimally insert repeaters to minimize the sum of the delay values of the nets. However, you should also minimize the total area. Find an optimal solution that minimizes the sum of the delay values and the total area. Notice that minimizing the total delay has a higher priority. Thus, if there exists only one solution that minimizes the total delay, find it. If there exist multiple solutions that minimize the total delay, find the smallest-area solution among them.

Let the k-th repeater of net 1 be $R_{1,k}$ and the k-th repeater of net 2 be $R_{2,k}$.

Minimization of the sum of the delays requires aligning the polarities of the signals. Thus, let $R_{1,1}$ be an inverter and $R_{2,1}$ be a buffer. Then, the signals are aligned after the first repeater. Now, we insert inverters after them to reduce the total area, i.e., $R_{1,2}, R_{1,3}, R_{1,4}, R_{1,5}, R_{2,2}, R_{2,3}, R_{2,4}, R_{2,5}$ are inverters. To satisfy the signal inversion constraint, $R_{1,6}$ should be an inverter and $R_{2,6}$ should be a buffer. Then, the sum of the delays of net 1 is $2d + 5 * d + 2d = 9d$ and the total delay is $14S$.

Problem #7 (CMOS Gates, 10 points).



What does the above circuit do? Describe the function of the circuit in as much detail as possible (A, B, C: input, Out: output).

If $C = 0$, the output is floating (tri-state).

Suppose $C = 1$. If $B = 0$, input A is blocked and C holds the last value of input A.

If $C = 1$ and $B = 1$, input A is transferred to the output.

Thus, this is a tri-state active-low D latch.

Problem #8 (Adder, 10 points).

Draw a gate-level schematic of a four-bit conditional sum adder (use full adders and muxes). Input: A[3:0], B[3:0], CI. Output: S[3:0], CO.