

# EE434

## ASIC and Digital Systems

### Midterm Exam 1

March 7, 2015. (5:10pm – 6pm)

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**Name:**

**WSU ID:**

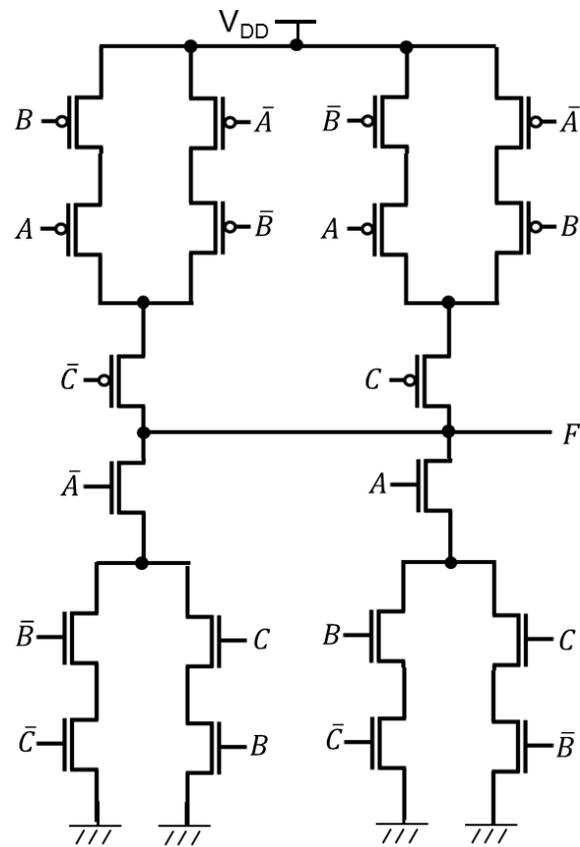
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
Total	80	

\* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

\* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

### Problem #1 (Static CMOS gates, 10 points).

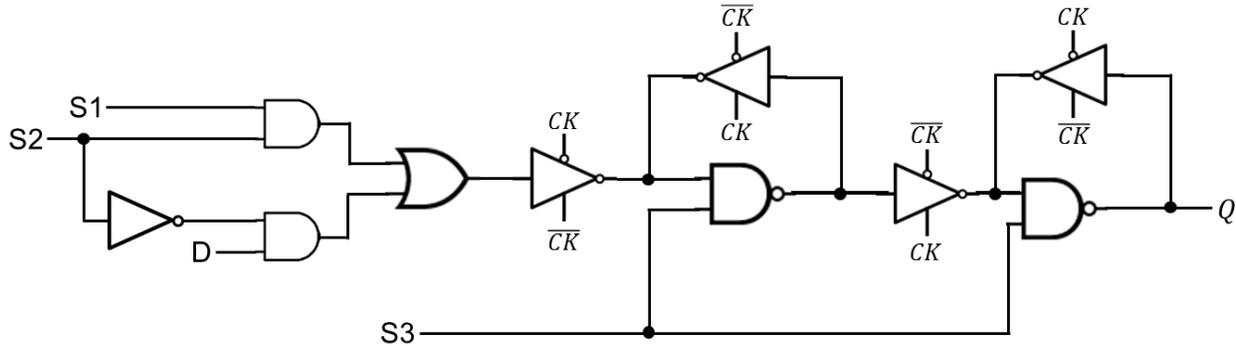
Represent  $F$  as a Boolean function of  $A, B,$  and  $C$ .



$$\begin{aligned}
 F &= \overline{\bar{A} \cdot (\bar{B} \cdot \bar{C} + B \cdot C) + A \cdot (B \cdot \bar{C} + \bar{B} \cdot C)} = \overline{\bar{A} \cdot (\overline{B \oplus C}) + A \cdot (B \oplus C)} = \overline{\overline{\bar{A} \oplus (B \oplus C)}} \\
 &= A \oplus B \oplus C
 \end{aligned}$$

## Problem #2 (Static CMOS gates, 10 points).

What does the following circuit do? Describe the function of the circuit in as much detail as possible (CK is a clock signal).



1) When  $S3=0$ :  $Q=1$  regardless of all other signals.  $\Rightarrow$  S3 is an active-low set signal.

2) When  $S3=1$ ,  $S2=0$ :  $S1 \cdot S2 = 0$ , so the output of the OR gate is D. The rest of the circuit is just a positive edge-triggered D-FF in this case (Q captures D at each clock rising edge).

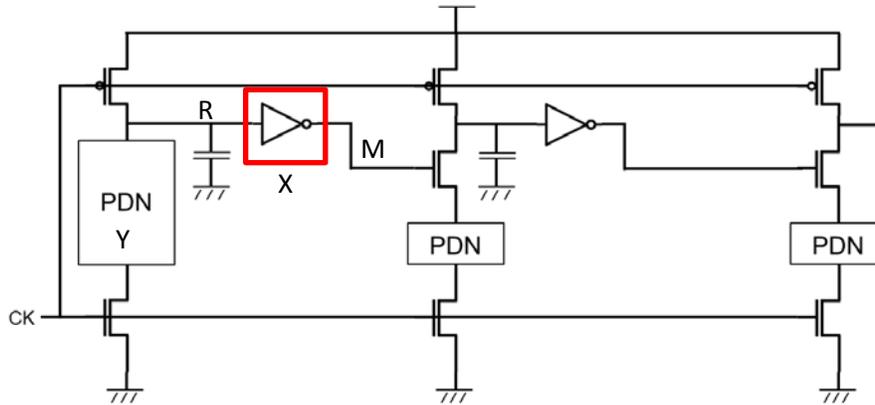
3) When  $S3=1$ ,  $S2=1$ : The output of the OR gate is S1. The rest of the circuit is just a positive edge-triggered D-FF (Q captures S1 at each clock rising edge).

From this, we can conclude that this is a positive edge-triggered D-FF with an asynchronous active-low set and two inputs (D is selected when  $S2=0$  and S1 is selected when  $S2=1$ ).

For your information, this is a positive edge-triggered D-FF with an asynchronous active-low set, a scan input (S1), and an active-high scan enable (S2).

### Problem #3 (Domino Logic and DC Characteristics, 10 points).

The following shows a general three-stage domino logic. When CK is 0, the logic precharges all internal nodes, so node R is 1 and node M is 0. In general, the PMOS transistors for precharging are properly upsized. When CK is 1, the logic evaluates the PDNs. When the PDN Y is true, it discharges node R, so R becomes 0 and M becomes 1. However, the PDNs in the logic are cascaded, so the PDNs should switch quite fast. Thus, the NMOS transistors in the PDNs are also properly upsized.



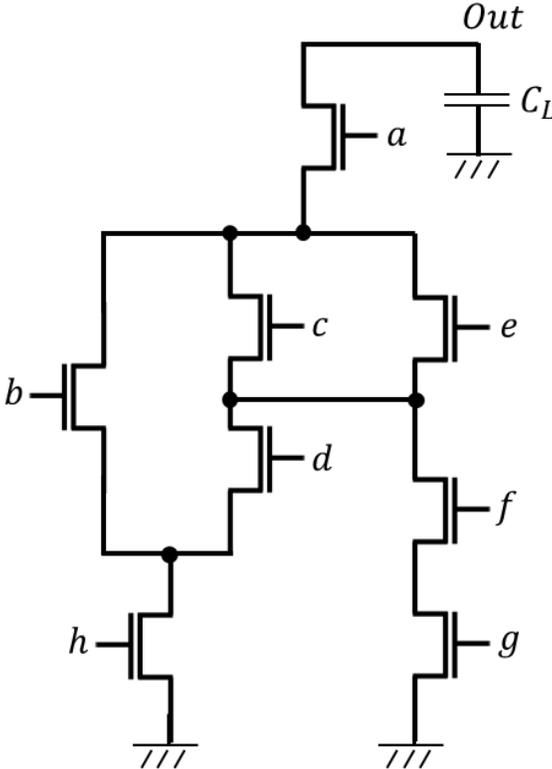
The NMOS transistor of inverter X can be small because it is used to discharge node M, which has a sufficiently small capacitance, during precharging. However, the PMOS transistor of inverter X should be properly upsized (e.g., by 16X) because it is used to charge node M during evaluation, so its switching time should be very short.

Question) Does this size imbalance (e.g., NMOS: 1X, PMOS: 16x) of inverter X cause any DC characteristics (noise margin) problems for inverter X? Explain why it causes (or does not cause any) DC characteristics (noise margin) problems for inverter X.

Yes, it causes some problems. When the PMOS transistor of inverter X is much larger than the NMOS transistor of inverter X, the DC characteristic curve of inverter X shifts to the right. In this case,  $NM_H = |V_{OH} - V_{IH}|$  significantly decreases (because  $V_{IH}$  goes up), but  $NM_L = |V_{IL} - V_{OL}|$  significantly increases (because  $V_{OL}$  goes up). Thus, we have some problems in the high noise margin. For instance, if PDN Y is false, R is 1, so M should be 0. However, if some noise signals affect node R or small charge sharing happens between R and an internal node in PDN Y, R will be slightly less than  $V_{DD}$ , which could invert the output of inverter X when PDN Y is false.

**Problem #4 (Transistor Sizing, 10 points).**

Size the transistors in the following pull-down network.  $R_n$  is the resistance of a 1X NMOS transistor. Ignore parasitic capacitances. Target time constant:  $\tau_{target} = R_n \cdot C_L$ . Try to minimize the total area.



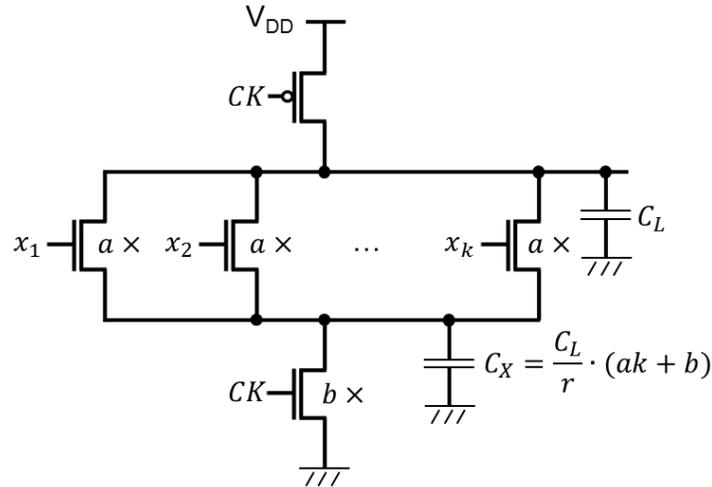
The worst-case path: (a-e-f-g) or (a-e-d-h) or (a-c-f-g) or (a-c-d-h), so we upsize all these transistors by 4X. Path (a-b-h) needs to be  $R_n$ , so b can be 2X.

a, c, d, e, f, g, h: 4X

b: 2X

## Problem #5 (Transistor Sizing, 10 points).

We want to design a  $k$ -input NOR gate. However, the static CMOS gate design methodology is not suitable for the design of the  $k$ -input NOR gate. Thus, we are going to design it using the dynamic CMOS design methodology. The following shows a schematic of the  $k$ -input NOR gate.



$R_n$  is the resistance of a 1X NMOS transistor. Target time constant:  $\tau_{target} = R_n \cdot C_L$ . All the transistors for  $x_1 \sim x_k$  are upsized to  $aX$  and the NMOS transistor for  $CK$  is upsized to  $bX$  ( $a$  and  $b$  are **real** numbers). Unfortunately, the parasitic capacitance at the internal node shown above is proportional to the sum of the width of the transistors connected to the node. Thus, the parasitic capacitance  $C_X$  at the internal node is  $C_X = \frac{C_L}{r} \cdot (ak + b)$  where  $C_L$  is the load cap and  $r$  is a constant ( $r > 1$ ). We minimize the total width

$$Width = a \cdot k + b.$$

Find  $a$  minimizing the total width (i.e., represent  $a$  as a function of  $k$  and  $r$ ).

$$\text{Constraints: } \left(\frac{R_n}{a} + \frac{R_n}{b}\right) \cdot C_L + \frac{R_n}{b} \cdot C_X = R_n \cdot C_L \Rightarrow \left(\frac{1}{a} + \frac{1}{b}\right) + \frac{ak+b}{br} = 1 \Rightarrow$$

$$\begin{aligned} \frac{1}{a} + \frac{1}{b} + \frac{1}{r} + \frac{ak}{br} = 1 &\Rightarrow \frac{1}{b} \left(1 + \frac{ak}{r}\right) = 1 - \frac{1}{a} - \frac{1}{r} = \frac{ar - a - r}{ar} \Rightarrow \frac{1}{b} \\ &= \frac{ar - a - r}{ar} \cdot \frac{r}{ak + r} = \frac{ar - a - r}{ka^2 + ra} \Rightarrow b = \frac{ka^2 + ra}{(r-1)a - r} \end{aligned}$$

$$\text{Minimize } W = ak + b = ak + \frac{ka^2 + ra}{(r-1)a - r}$$

$$W' = k + \frac{(2ka + r)((r-1)a - r) - (ka^2 + ra)(r-1)}{\{(r-1)a - r\}^2}$$

$$= k + \frac{\{2k(r-1)a^2 - 2kra + r(r-1)a - r^2\} - \{k(r-1)a^2 + r(r-1)a\}}{\{(r-1)a - r\}^2}$$

$$= k + \frac{k(r-1)a^2 - 2kra - r^2}{\{(r-1)a - r\}^2}$$

$$= \frac{k(r-1)^2a^2 - 2kr(r-1)a + kr^2 + k(r-1)a^2 - 2kra - r^2}{\{(r-1)a - r\}^2}$$

$$= \frac{kr(r-1)a^2 - 2kr^2a + kr^2 - r^2}{\{(r-1)a - r\}^2} = \frac{kr(r-1)a^2 - 2kr^2a + (k-1)r^2}{\{(r-1)a - r\}^2}$$

$$W' = 0 \Rightarrow a = \frac{kr^2 \pm \sqrt{k^2r^4 - k(k-1)(r-1)r^3}}{kr(r-1)}$$

$$= \frac{kr^2 \pm \sqrt{k^2r^4 - (k^2r^4 - k^2r^3 - kr^4 + kr^3)}}{kr(r-1)} = \frac{kr^2 \pm \sqrt{k^2r^3 + kr^4 - kr^3}}{kr(r-1)}$$

$W$  is minimized when

$$a = \frac{kr^2 + \sqrt{k^2r^3 + kr^4 - kr^3}}{kr(r-1)}$$

Quick double check:

1) When  $r \rightarrow \infty$  (i.e.,  $C_X$  is negligible),  $a \rightarrow \frac{k+\sqrt{k}}{k} = 1 + \frac{1}{\sqrt{k}}$

$\frac{1}{a} + \frac{1}{b} = 1$ , so  $\frac{1}{b} = 1 - \frac{k}{k+\sqrt{k}} = \frac{\sqrt{k}}{k+\sqrt{k}} \Rightarrow b \rightarrow 1 + \sqrt{k}$  (which is an answer we obtain when we ignore  $C_X$ ).

For example, if  $k = 1$  (just a two-input NOR ignoring  $C_X$ ),  $a = b = 2$ .

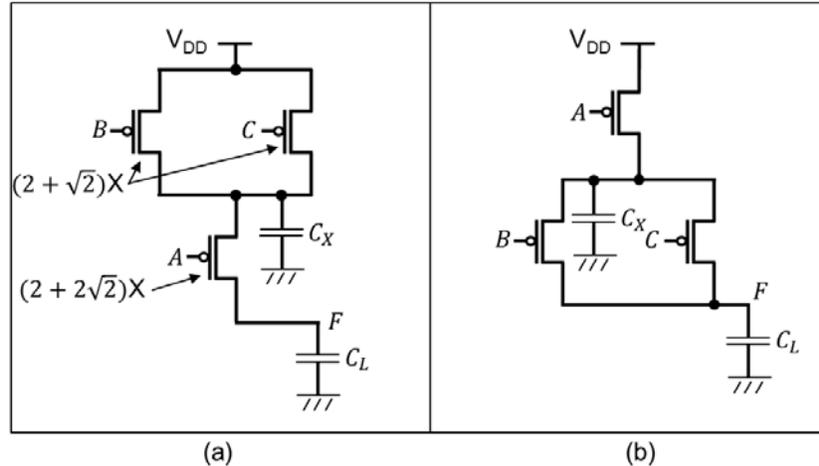
2) When  $r \rightarrow 1$  (i.e.,  $C_X \gg C_L$ ),  $a = \frac{k+\sqrt{k^2}}{k(r-1)} = \frac{2}{r-1}$

$$\frac{1}{a} + \frac{1}{b} + \frac{ak}{b} = \frac{r-1}{r}, \text{ so } \frac{1}{b}(1+ak) = \frac{r-1}{r} - \frac{1}{a} \Rightarrow \frac{1}{b} = \frac{r-1}{2r(1+ak)} \Rightarrow b = \frac{2r}{r-1} \left(1 + \frac{2k}{r-1}\right)$$

In this case, we are supposed to upsize  $a$  to  $(2 + \delta)X$  where  $\delta$  is a very small positive number and  $b$  to a large number. This makes sense because the fall time is dominated by the internal cap, so we need to upsize the CK NMOS transistor. (However,  $x_i$  should be up-sized by  $(2 + \delta)X$ , otherwise you won't be able to achieve the target time constant).

## Problem #6 (Switching Characteristics, 10 points).

We design  $F = \overline{A + B \cdot C}$  using the static CMOS gate design style. The following shows a transistor-level schematic of the pull-up network of the design:



Both (a) and (b) are functionally equal. The internal node in the pull-up network has parasitic capacitance  $C_X$ . Since the parasitic capacitance of an internal node is generally determined by the size of the transistors connected to the node, both (a) and (b) have the same parasitic capacitance  $C_X$ .  $R_n$  is the resistance of a 1X NMOS transistor.  $\mu_n = 2\mu_p$ . Target time constant:  $\tau_{target} = R_n \cdot C_L$ . If we optimally size the pull-up network to minimize the total width without considering  $C_X$ , the pMOS A is upsized to  $(2 + 2\sqrt{2})X$  and the pMOS B and C are upsized to  $(2 + \sqrt{2})X$  as shown in the figure.

Compute the worst-case rise time in (a) and in (b) considering  $C_X$ , i.e., represent the worst-case rise time as a function of  $R_n$ ,  $C_L$ , and  $C_X$ . Which design has shorter rise time?

$$(a) \text{ Worst cases: } (A, B, C) = (0, 0, 1) \text{ or } (0, 1, 0). R_B = R_C = \frac{R_p}{2+\sqrt{2}} = \frac{2R_n}{2+\sqrt{2}}, R_A = \frac{R_p}{2+2\sqrt{2}} = \frac{2R_n}{2+2\sqrt{2}} = \frac{R_n}{1+\sqrt{2}}$$

$$\tau_a = R_B \cdot C_X + (R_B + R_A) \cdot C_L = \frac{2R_n}{2+\sqrt{2}} \cdot C_X + \left( \frac{2R_n}{2+\sqrt{2}} + \frac{R_n}{1+\sqrt{2}} \right) \cdot C_L$$

$$t_r = 2.2\tau_a$$

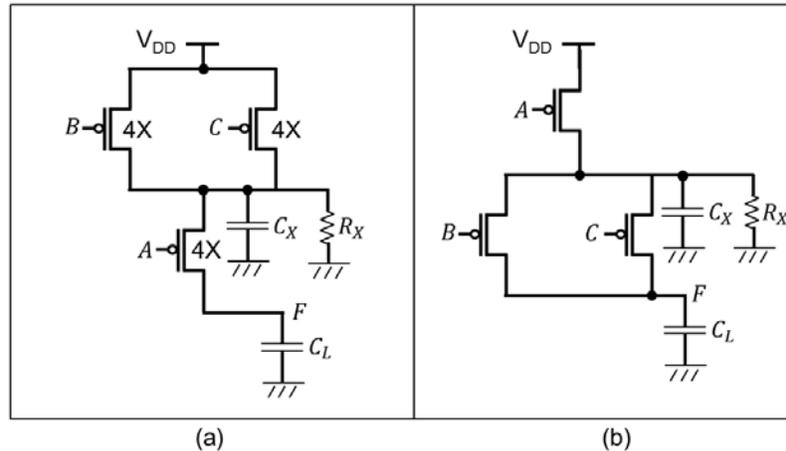
$$(b) \tau_b = R_A \cdot C_X + (R_A + R_B) \cdot C_L = \frac{R_n}{1+\sqrt{2}} \cdot C_X + \left( \frac{R_n}{1+\sqrt{2}} + \frac{2R_n}{2+\sqrt{2}} \right) \cdot C_L$$

$$t_r = 2.2\tau_b$$

I prefer design (b) because it has shorter rise time than (a).

## Problem #7 (Power Consumption, 10 points).

We design  $F = \overline{A + B \cdot C}$  using the static CMOS gate design style. The following shows a transistor-level schematic of the pull-up network of the design:



Both (a) and (b) are functionally equal. The internal node in the pull-up network has parasitic capacitance  $C_X$  and also a parasitic resistance  $R_X$  connected to the ground (this is a leaky path, i.e., even if  $A=B=C=1$  and  $C_X = V_{DD}$ ,  $C_X$  will be slowly discharged through  $R_X$ ). All the transistors are upsized by 4X as shown in the figure. The following table shows the probability that each input signal is 0 or 1:

	0	1
A	0.8	0.2
B	0.2	0.8
C	0.2	0.8

We want to minimize power consumption (both dynamic and leakage power) of the gate. Which design do you prefer? (a) or (b)? Select one of them and explain why you prefer the design to minimize power consumption. You can qualitatively and intuitively explain it (without performing accurate probability and power computation).

I would prefer design (a). In (b), A is frequently set to 0, so  $C_X$  will be frequently charged and leak through  $R_X$ . In (a), however, B and C are less frequently set to 0, so it will charge  $C_X$  less frequently than (b). Thus, we can minimize leakage power. However, both (a) and (b) consume the same amount of dynamic power.

