EE434

ASIC and Digital Systems

Midterm Exam 1

Feb. 22, 2017. (4:10pm – 5pm)

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Name:

WSU ID:

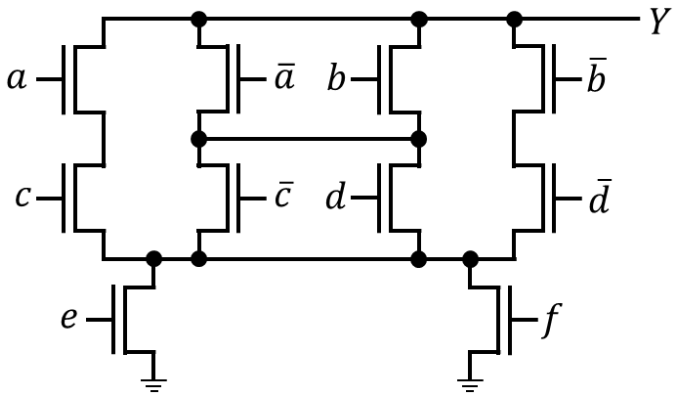
Problem	Points	
1	10	
2	10	
3	10	
4	20	
5	10	
Total	60	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Static CMOS gates, 10 points).

The pFET network of the following nFET network is designed by the dual network of the nFET network. Represent Y as a Boolean function of a, b, c, d, e and f. (Try to simplify the Boolean function).

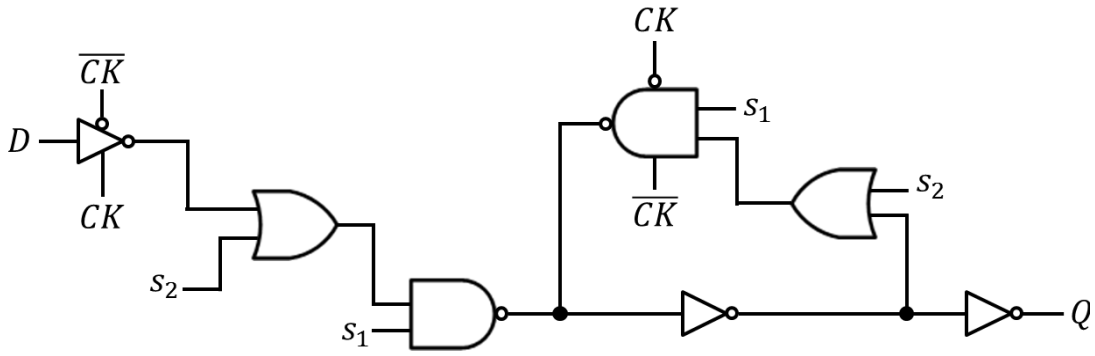


Problem #2 (Analysis of CMOS gates, 10 points).

The following circuit is a sequential logic. Describe the function of the circuit in as much detail as possible (D: data input, CK: clock, s_1, s_2: control inputs).

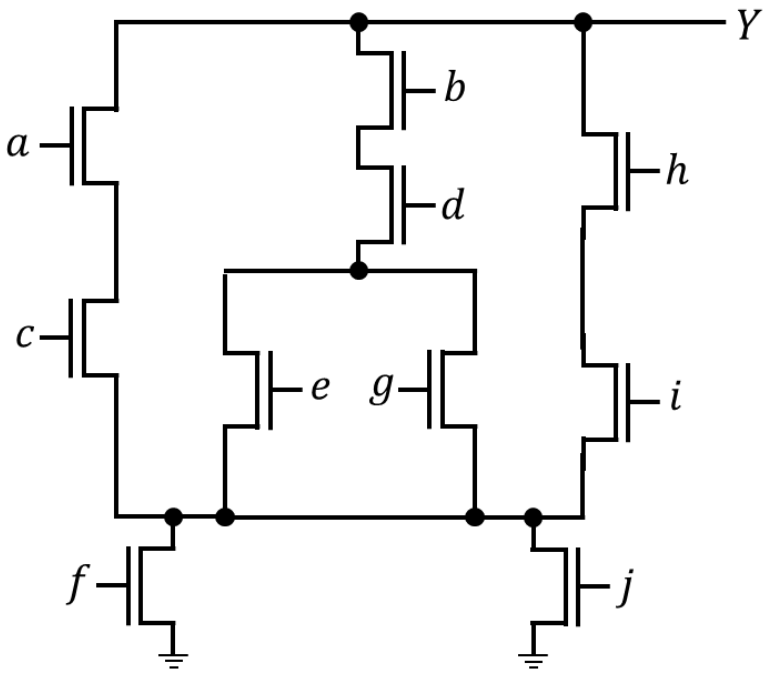
Note:

- Logic
  - F/F vs. Latch
  - Positive-edge triggered vs. Negative-edge triggered (for F/F)
  - Active-high vs. Active-low (for Latch)
- Control inputs
  - Asynchronous vs. Synchronous
  - Active-high vs. Active-low
  - Set, Reset, Enable, Select, Additional input
  - Dominance (e.g., Set dominates Reset, Enable dominates Set, etc.)



Problem #3 (Transistor Sizing, 10 points).

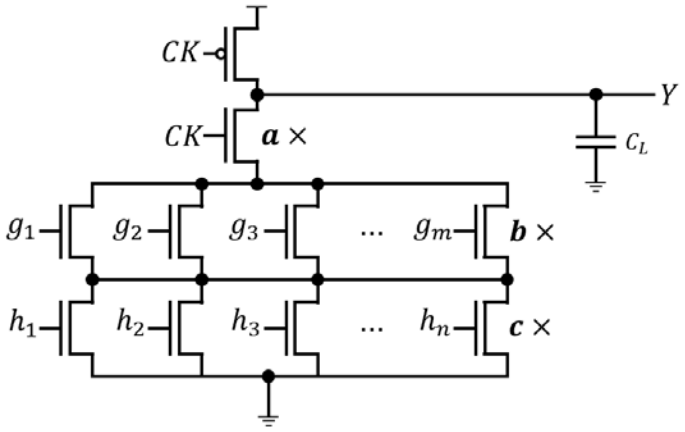
Size the transistors in the following pull-down network. R_n is the resistance of a 1X NMOS transistor. Ignore parasitic capacitances. Target time constant: $\tau_{target} = R_n \cdot C_L$. Try to minimize the total area.



a:
b:
c:
d:
e:
f:
g:
h:
i:
j:

Problem #4 (Transistor Sizing, 20 points).

We want to design the following logic: $Y = \overline{(g_1 + g_2 + \cdots + g_m) \cdot (h_1 + h_2 + \cdots + h_n)}$ where $g_1 \sim g_m$ and $h_1 \sim h_n$ are the inputs of the gate. However, the static CMOS gate design methodology is not suitable for the design of the gate. Thus, we are going to design it using the dynamic CMOS design methodology. The following shows a schematic of the gate.



R_n is the resistance of a 1X nFET. Target time constant: $\tau_{target} = R_n \cdot C_L$. The nFET connected to CK is upsized to $\boldsymbol{a}$ ×, all the nFETs connected to $g_1 \sim g_m$ are upsized to $\boldsymbol{b}$ ×, and all the nFETs connected to $h_1 \sim h_n$ are upsized to $\boldsymbol{c}$ × to satisfy the timing constraint (a, b, c are real numbers). Ignore all the parasitic capacitance. We ***minimize*** the total width

$$Width = a + m \cdot b + n \cdot c.$$

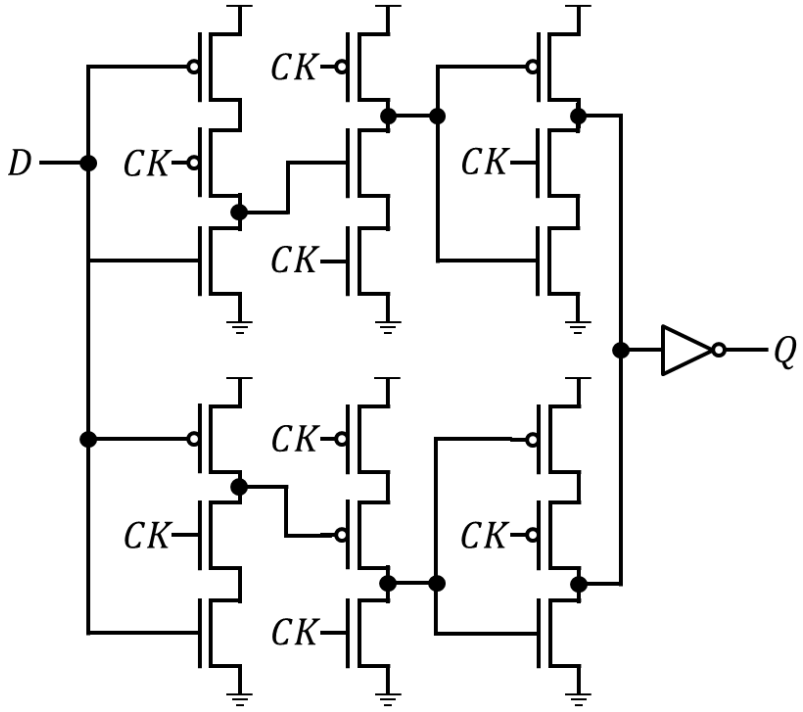
Problem 4-1 (8 points): Find $a, b,$ and c minimizing the total width (i.e., represent each of $a, b,$ and c as a function of n and m).

Problem 4-2 (12 points, True/False. Use your intuition or the formulas you derived in the above problem).)

- If we increase n, a increases. (True / False)
- If we increase m, a increases. (True / False)
- If we increase n, b increases. (True / False)
- If we increase m, b increases. (True / False)
- If we increase n, c increases. (True / False)
- If we increase m, c increases. (True / False)

Problem #5 (Logic Analysis, 10 points).

What does the following circuit do? Describe the function of the circuit in as much detail as possible (CK is a clock signal, D is an input, Q is an output). Note: if a node is floating, it holds its previous value.



(M. Afghahi, JSSC'91)