EE434

ASIC and Digital Systems

Midterm Exam 2

Mar. 31, 2017. (4:10pm – 5pm)

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Name:

WSU ID:

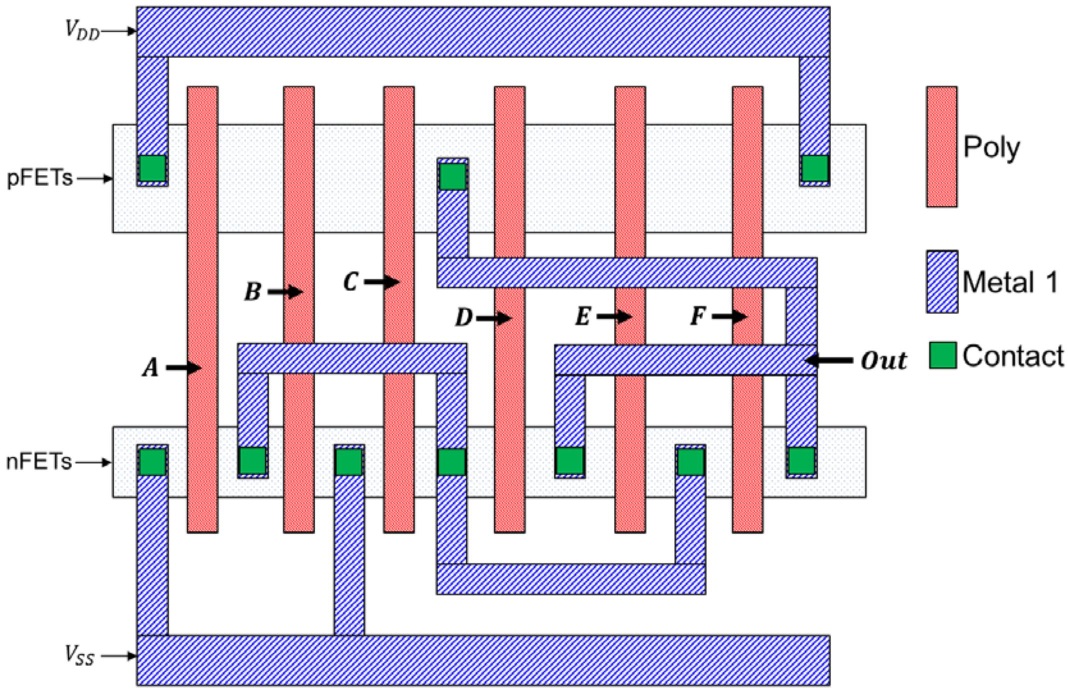
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
Total	50	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

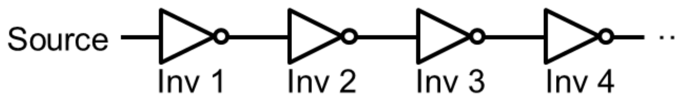
Problem #1 (Layout, 10 points).

Represent Out as a Boolean function of A, B, C, D, E, F.

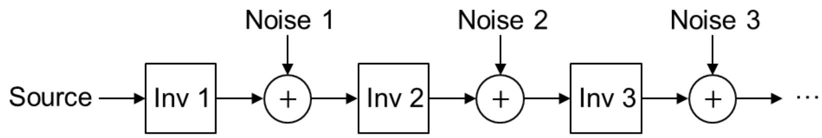


Problem #2 (DC Characteristics, 10 points).

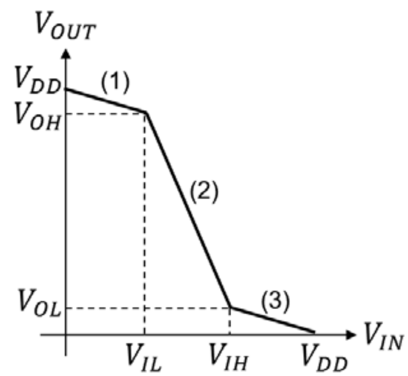
An infinite chain of inverters is defined as follows:



All the inverters are identical, i.e., have the same characteristics. The above chain is modeled as a block diagram as follows:



where $Noise\ k$ is the k-th noise and $Source$ is a signal generator and $V_{Source} = V_{DD} \cdot u(t)$ (i.e., 0 if $t < 0$ and V_{DD} if $t \geq 0$). $V_{DD} = 1V$. The DC characteristic of an inverter is approximated using three segments as follows (If $V_{in} \geq V_{DD}, V_{out} = 0$. If $V_{in} \leq 0, V_{out} = V_{DD}$.):



1) $\boldsymbol{V_{out}} = \frac{V_{OH}-V_{DD}}{V_{IL}} \cdot \boldsymbol{V_{in}} + V_{DD}$
2) $\boldsymbol{V_{out}} = \frac{V_{OL}-V_{OH}}{V_{IH}-V_{IL}} \cdot (\boldsymbol{V_{in}} - V_{IH}) + V_{OL}$
3) $\boldsymbol{V_{out}} = -\frac{V_{OL}}{V_{DD}-V_{IH}} \cdot (\boldsymbol{V_{in}} - V_{DD})$

Each noise source is an independent voltage signal and its range is as follows ($V_N > 0$):

- $|V_{noise}| \leq V_N$

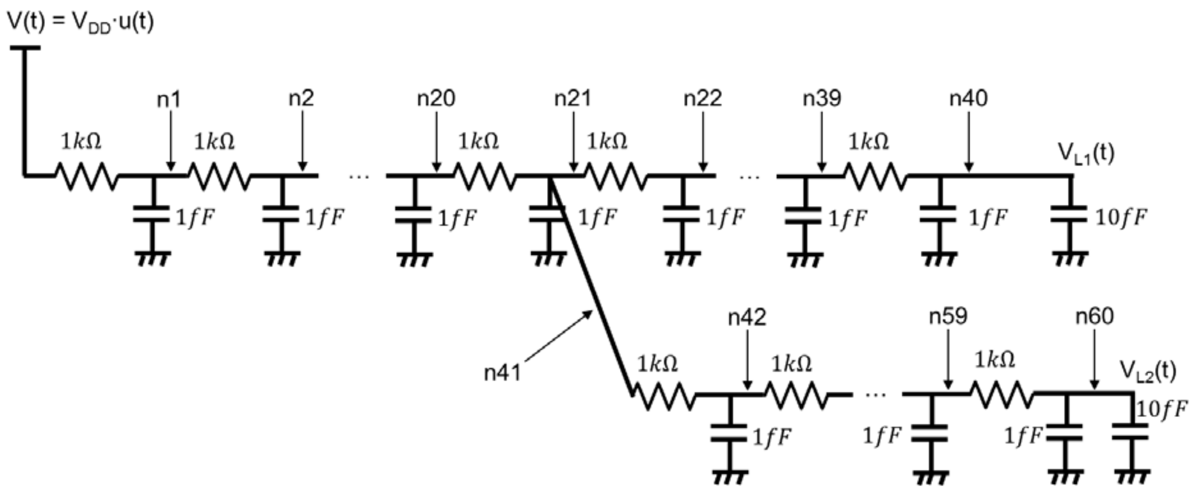
<u>Compute the max. value of V_N that does not cause signal inversion for the following two cases (Note: Signal inversion occurs if a signal reaches 0.5V when it should be 0 or 1):</u>

- Case 1) $V_{OL} = 0V, V_{OH} = 1V, V_{IL} = 0.4V, V_{IH} = 0.6V$
- Case 2) $V_{OL} = 0V, V_{OH} = 1V, V_{IL} = 0.4V, V_{IH} = 0.8V$

Problem #3 (Elmore Delay, 10 points).

The RC tree shown below has two delay constraints as follows:

- The delay from the driver to V_{L1} should be less than or equal to $900ps$.
- The delay from the driver to V_{L2} should be less than or equal to $6823ps$.

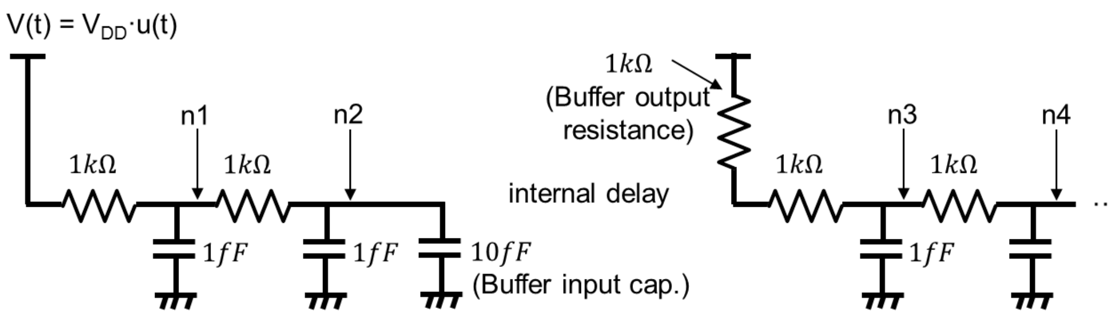


Currently, the delay at V_{L1} is $1k * 11f + 1k * 12f + \cdots + 1k * 29f + 1k * 59f + 1k * 60f + \cdots + 1k * 79f = 1829ps$, so is the delay at V_{L2}.

You are supposed to insert <u>*only one buffer*</u> in the RC tree to satisfy the delay constraints at both V_{L1} and V_{L2}. You can insert the buffer only into one of the designated nodes (n1 ~ n60). The buffer has the following characteristics:

- Input capacitance: $10fF$
- Internal delay: $20ps$
- Output resistance: $1k\Omega$

When you insert a buffer into a node, the RC tree before and after the buffer are separated as follows (assuming the buffer is inserted into n2 in the figure above):



In this case (inserting a buffer into n2), the delay at V_{L1} is $[1k * 11f + 1k * 12f + \cdots + 1k * 29f + 1k * 59f + 1k * 60f + \cdots + 1k * 77f + 1k * 77f] + [20ps] + [1k * 11f + 1k * 12f] = (1749 + 20 + 23)ps = 1792ps$, so is the delay at V_{L2}. As you see, the delay is reduced from $1829ps$ to $1792ps$.

Insert a buffer into one of the nodes (n1 ~ n60) so that it satisfies the delay constraints at both V_{L1} and V_{L2}. Then, compute the Elmore delay at V_{L1}.

(Help: The sum of $a, a+1, a+2, \ldots, n$ is $\frac{(n+a)(n-a+1)}{2}$. For example, $5 + 6 + \cdots + 10 = \frac{(10+5)(10-5+1)}{2} = 45$.)

Node:

Elmore delay at V_{L1}:

Problem #4 (Pseudo-nMOS, 10 points).

Draw a pseudo-nMOS schematic for $Y = \overline{A \cdot B \cdot C + (D + E) \cdot F}$ and properly size the nFETs to achieve the following output level for logic output 0:

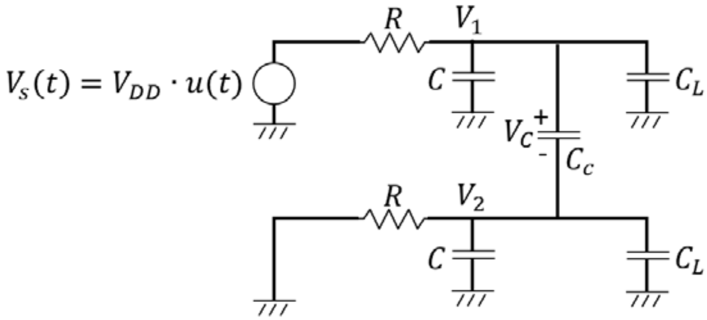
- $V_{out} \leq 0.1V_{DD}$

Use the following parameters:

- Resistance of a $1 \times$ nFET = Resistance of a $2 \times$ pFET
- The size of the pFET: $4 \times$
- Do not use the transistor-mode-based computation for sizing. You can just use the resistance values for sizing.
- Do not oversize the nFETs.

Problem #5 (Capacitive Coupling, 10 points).

The following figure models the coupling effect between two adjacent wires.



$V_1(t)$ is an aggressor and $V_2(t)$ is a victim. $V_2(t)$ is as follows:

$$V_2(t) = \frac{V_{DD}}{2}\left[e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}\right]u(t)$$

where

- $\boldsymbol{\tau_1 = R(C + C_L + 2C_C)}$
- $\boldsymbol{\tau_2 = R(C + C_L)}$

In this case, the max. value of $V_2(t)$ is found by differentiating $V_2(t)$ with respect to t. The max. value occurs when t is

$$t_{max} = \frac{R(C + C_L)(C + C_L + 2C_C)}{2} \cdot \ln\frac{C + C_L + 2C_C}{C + C_L}$$

and the max. value of $V_2(t)$ is

$$\boldsymbol{V_{2,max} = \frac{V_{DD}}{2} \cdot \left(1 - \frac{\tau_2}{\tau_1}\right) \cdot \left(\frac{\tau_2}{\tau_1}\right)^{\frac{\tau_2}{2RC_C}}}$$

Answer the following questions (Hint: Use the above formula or your intuition to solve this problem):

- If C_C increases, $V_{2,max}$ increases. (True/False)
- If C increases, $V_{2,max}$ increases. (True/False)
- If C_L increases, $V_{2,max}$ increases. (True/False)
- If R increases, $V_{2,max}$ increases. (True/False)
- The max. value of $V_2(t)$ can be greater than $V_{DD}/2$. (True/False)

(Hint: $\lim_{x\to\infty}\left(\frac{1}{x}\right)^{\frac{1}{x}}=1$. $\lim_{x\to\infty}\left(\frac{x}{x+c}\right)^{\frac{x}{c}}=e$. $\left(\frac{x}{x+c}\right)^{\frac{x}{c}}>1$. (when $c>0$))