EE434

ASIC and Digital Systems

Midterm Exam 1

Feb. 16, 2018. (4:10pm – 5pm)

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Name:

WSU ID:

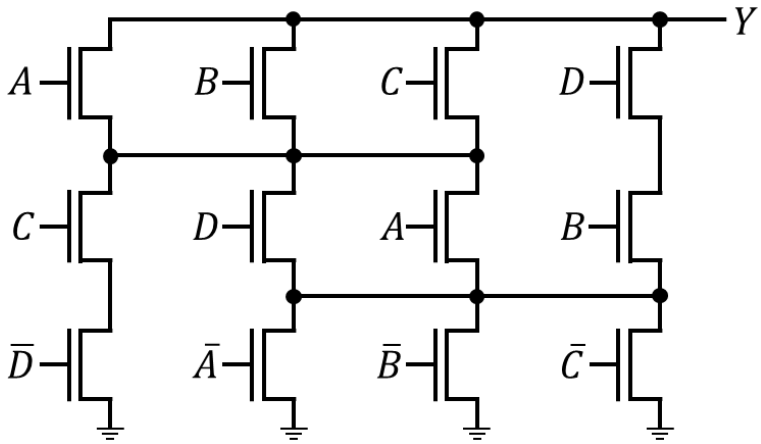
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
Total	60	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

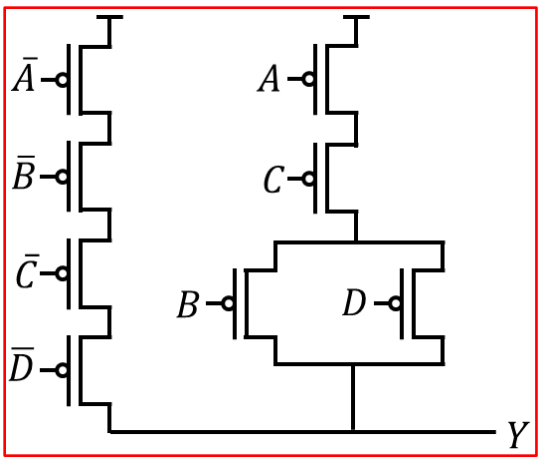
Problem #1 (Static CMOS gates, 10 points)

The following shows the NFET network of a static CMOS gate. Draw a PFET network for the gate. Available inputs: $A, B, C, D, \bar{A}, \bar{B}, \bar{C}, \bar{D}$. You should minimize the total number of PFETs in your PFET network.



A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Thus, Y is 1 in the following four cases: $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + ABCD = ABCD + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{C}\bar{D} = ABCD + \bar{A}\bar{C}(\bar{B} + \bar{D})$.

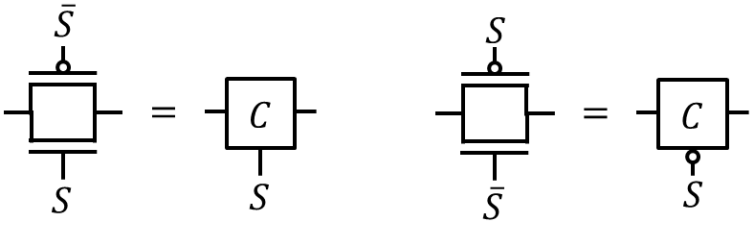

$\bar{A}$
$\bar{B}$
$\bar{C}$
$\bar{D}$
A
C
B
D
Y

Problem #2 (Transmission Gates, 10 points)

Design (draw a schematic) the following Boolean function using transmission gates only.

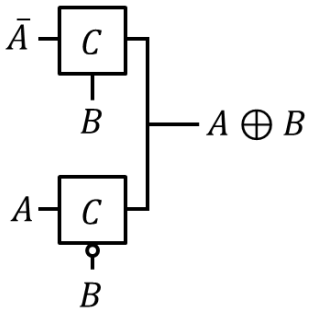
$$Y = A \oplus B \oplus C$$

Available inputs: $A, B, C, \bar{A}, \bar{B}, \bar{C}$. You cannot use Power ($V_{DD}$) and Ground ($V_{SS}$). Use the following symbols for the transmission gates.

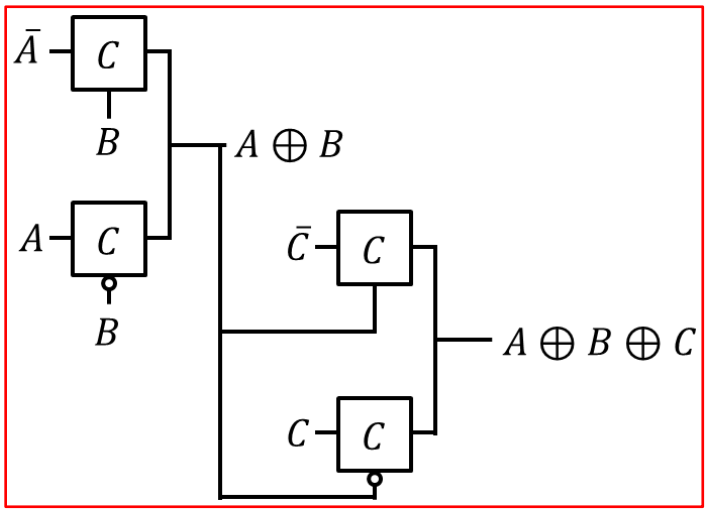


Design constraint: The total # transmission gates should be less than or equal to 10.

$$F = A \oplus B = A\bar{B} + \bar{A}B$$



$$Y = (A \oplus B) \oplus C = F\bar{C} + \bar{F}C$$

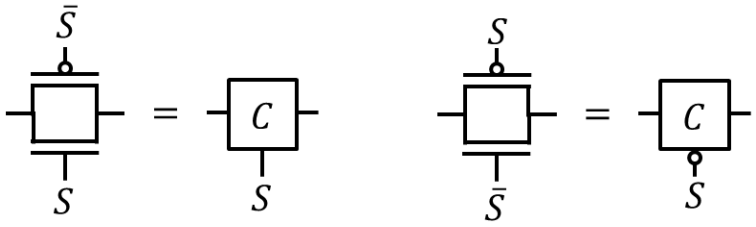


Problem #3 (Design, 10 points)

Design (draw a schematic) a two-bit comparator using transmission gates only. The following shows a truth table for the comparator:

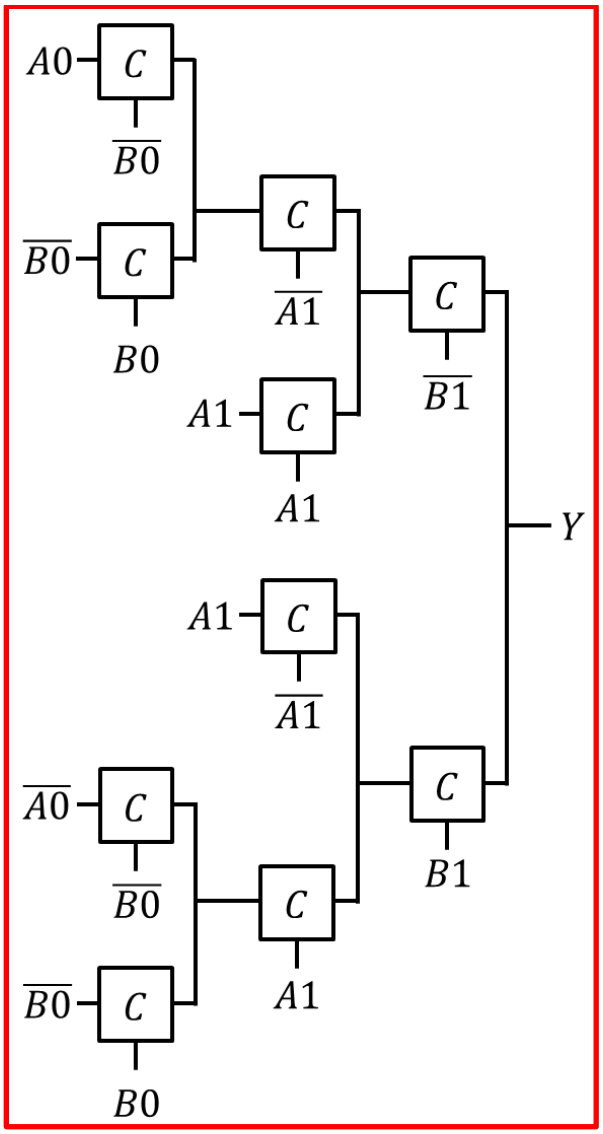
A1	A0	B1	B0		Y1
0	0	0	0		0
0	0	0	1		0
0	0	1	0		0
0	0	1	1		0
0	1	0	0		1
0	1	0	1		0
0	1	1	0		0
0	1	1	1		0
1	0	0	0		1
1	0	0	1		1
1	0	1	0		0
1	0	1	1		0
1	1	0	0		1
1	1	0	1		1
1	1	1	0		1
1	1	1	1		0

Available inputs: $A1, A0, B1, B0, \overline{A1}, \overline{A0}, \overline{B1}, \overline{B0}$. You cannot use Power ($V_{DD}$) and Ground ($V_{SS}$). Use the following symbols for the transmission gates.



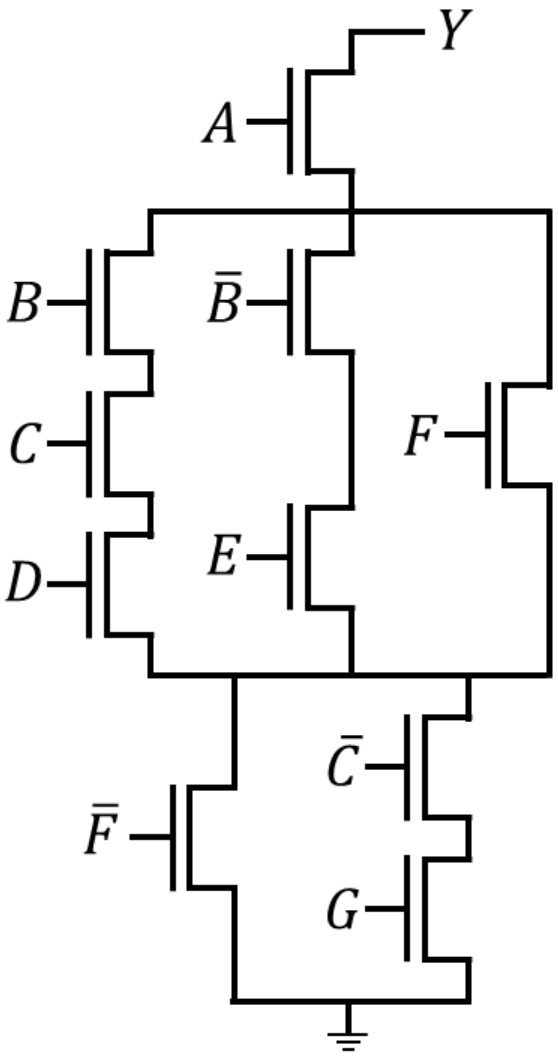
Design constraint: The total # transmission gates should be less than or equal to 12.

$$Y = A1 \cdot \overline{B1} + A0 \cdot \overline{B1} \cdot \overline{B0} + A1 \cdot A0 \cdot \overline{B0}$$


A0
C
$\overline{B0}$
$\overline{B0}$
C
B0
C
$\overline{A1}$
A1
C
A1
C
$\overline{B1}$
Y
A1
C
$\overline{A1}$
$\overline{A0}$
C
$\overline{B0}$
C
B1
$\overline{B0}$
C
B0
C
A1

Problem #4 (Transistor Sizing, 10 points).

Size the transistors in the following pull-down network. R_n is the resistance of a 1X NMOS transistor. Ignore parasitic capacitances. Target time constant: $\tau_{target} \leq R_n \cdot C_L$. Try to minimize the total area.



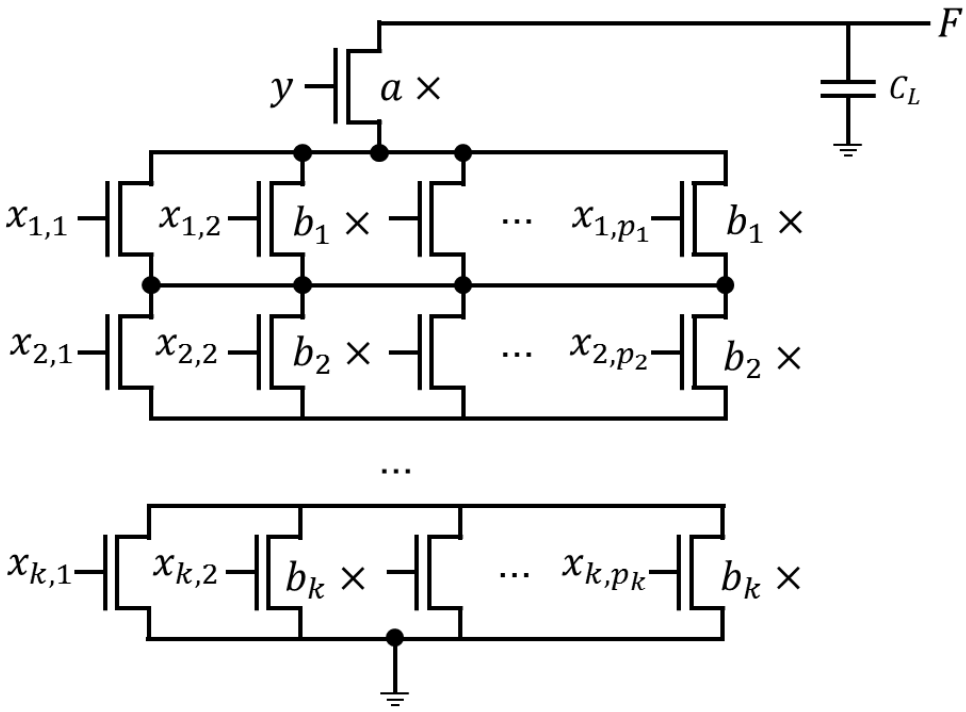
Paths $A - B - C - D - \bar{F}$ and $A - \bar{B} - E - \bar{C} - G$ are the two critical paths. Thus, we set the sizes of the NFETs on the path to 5X. To satisfy the timing constraint for the path $A - F - \bar{C} - G$, we set the size of the NFET F to 2.5X.

Total width: 47.5X

Problem #5 (Transistor Sizing, 10 points).

The following shows an NFET network of

$$F = \overline{y \cdot (x_{1,1} + \cdots + x_{1,p_1}) \cdot (x_{2,1} + \cdots + x_{2,p_2}) \cdot \ldots \cdot (x_{k,1} + \cdots + x_{k,p_k})}$$



Notice that $k, p_1, \ldots, p_k$ are constants. The fall delay should be less than or equal to $R_n C_L$ where R_n is the resistance of a 1 × NFET. The NFET y is upsized to a × and each NFET connected to $x_{i,j}$ is upsized to b_i ×. We <u>minimize</u> the total width

$$W = a + b_1 \cdot p_1 + b_2 \cdot p_2 + \cdots + b_k \cdot p_k.$$

<u>Find a (the size of the NFET connected to input y) that minimizes the total width (i.e., represent a as a function of $p_1, p_2, \ldots, p_k$.</u>

Timing constraint: $C_L(\frac{R_n}{a} + \frac{R_n}{b_1} + \frac{R_n}{b_2} + \cdots + \frac{R_n}{b_k}) \leq R_n C_L$. We take $=$, so the constraint is

$$\frac{1}{a} + \frac{1}{b_1} + \cdots + \frac{1}{b_k} = 1.$$

Substitution: $\frac{1}{a} = A, \frac{1}{b_i} = B_i$

$$A + \sum B_i = 1$$

$$W = a + \sum p_i b_i = \frac{1}{A} + \frac{p_1}{B_1} + \cdots + \frac{p_k}{B_k} = \frac{1}{1 - \sum B_i} + \sum \frac{p_i}{B_i}$$

$$\frac{\partial W}{\partial B_i} = \frac{1}{(1 - \sum B_i)^2} - \frac{p_i}{{B_i}^2} = 0$$

Substitution: $\sum B_i = S$

$$\frac{\partial W}{\partial B_i} = \frac{1}{(1-S)^2} - \frac{p_i}{{B_i}^2} = 0, so\ B_i = \sqrt{p_i}(1 - S).$$

$$\sum B_i = S = (1 - S) \sum \sqrt{p_i}$$

Substitution: $\sum \sqrt{p_i} = r$

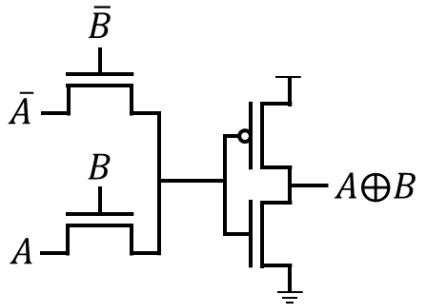
$$S = (1 - S)r, so\ S = \frac{r}{r+1}.$$

$$\therefore B_i = \frac{\sqrt{p_i}}{r+1} = \frac{\sqrt{p_i}}{1+\sum \sqrt{p_i}},\ b_i = \frac{1+\sum \sqrt{p_i}}{\sqrt{p_i}}$$

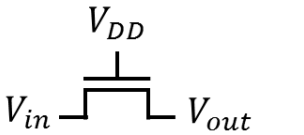
$$A = 1 - S = \frac{1}{r+1}, \therefore a = 1 + \sum \sqrt{p_i} = 1 + \sqrt{p_1} + \sqrt{p_2} + \cdots + \sqrt{p_k}$$

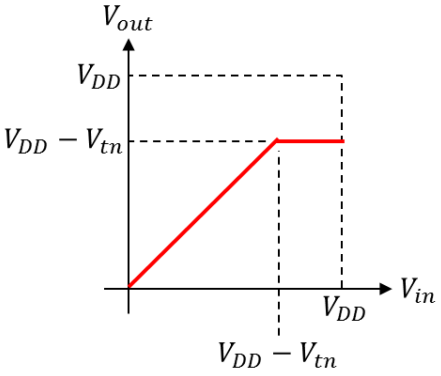
Problem #6 (Pass Transistor, 10 points)

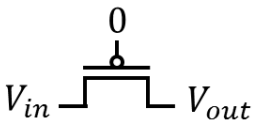
The following schematic implements an XOR gate using pass transistors.

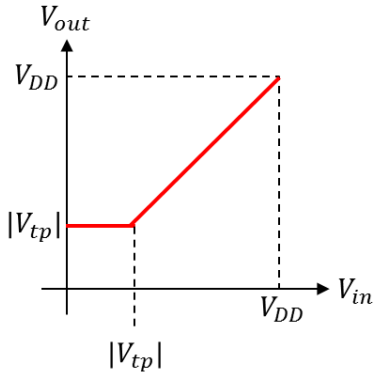


The inverter at the output restores the signal so that the output swing can be $[0, V_{DD}]$. The following plots show the V_{DS} characteristic of the NFET when its gate voltage is V_{DD} and the V_{DS} characteristic of the PFET when its gate voltage is 0.

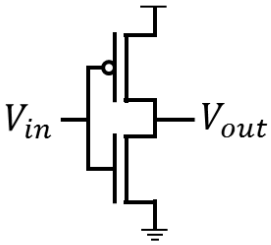


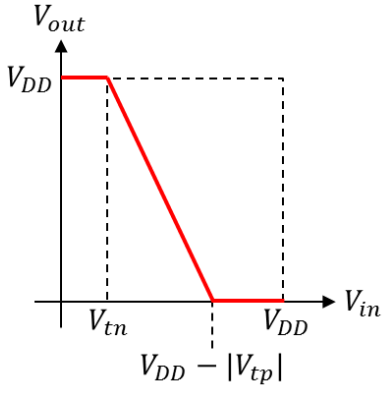






The following plot shows the input-output characteristic of the inverter.





V_{tn} and $|V_{tp}|$ are the threshold voltages of the NFET and the PFET, respectively. $A, B, \bar{A}, \bar{B}$ are either 0V (for 0) or V_{DD} (for 1). The swing of the final output $A \oplus B$ should be $[0, V_{DD}]$, i.e., 0V if $A \oplus B = 0$ and V_{DD} if $A \oplus B = 1$. Find all inequalities for the full output swing. (Hint: The inequalities might consist of V_{DD}, V_{tn}, and $|V_{tp}|$.)

A	B	Input of the inverter (logical)
0	0	$V_{DD} - V_{tn}$
0	1	0
1	0	0
1	1	$V_{DD} - V_{tn}$

Thus, if the input of the inverter is 0, the output voltage is V_{DD}. If the input is $V_{DD} - V_{tn}$, the output should be 0V. Thus, this should be greater than or equal to $V_{DD} - |V_{tp}|$. Thus, $V_{tn} \leq |V_{tp}|$ is the only inequality it should satisfy.