EE434

ASIC and Digital Systems

Midterm Exam 1

Feb. 16, 2018. (4:10pm – 5pm)

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Name:

WSU ID:

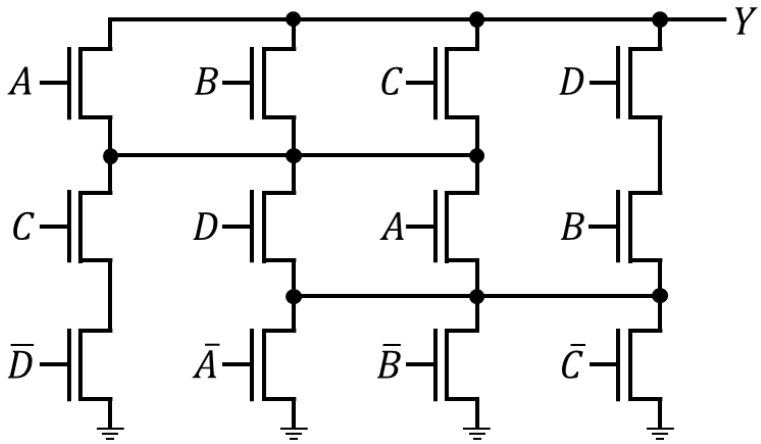
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
Total	60	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Static CMOS gates, 10 points)

The following shows the NFET network of a static CMOS gate. Draw a PFET network for the gate. Available inputs: $A, B, C, D, \bar{A}, \bar{B}, \bar{C}, \bar{D}$. You should minimize the total number of PFETs in your PFET network.



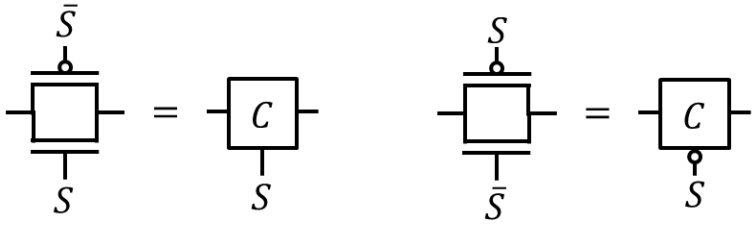
(# PFETs ≤10: 10 points. 11≤# PFETs≤12: 7 points. 13≤# PFETs≤14: 5 points. # PFETs>12: 0 points)

Problem #2 (Transmission Gates, 10 points)

Design (draw a schematic) the following Boolean function using transmission gates only.

$$Y = A \oplus B \oplus C$$

Available inputs: $A, B, C, \bar{A}, \bar{B}, \bar{C}$. You cannot use Power ($V_{DD}$) and Ground ($V_{SS}$). Use the following symbols for the transmission gates.



Design constraint: The total # transmission gates should be less than or equal to 10.

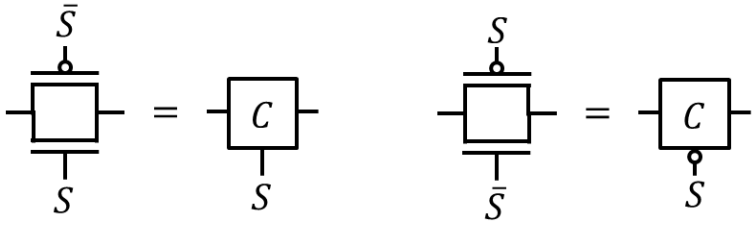
(# TGs≤10: 10 points. 11≤# TGs≤12: 7 points. 13≤# TGs≤14: 5 points. # TGs>14: 0 points)

Problem #3 (Design, 10 points)

Design (draw a schematic) a two-bit comparator using transmission gates only. The following shows a truth table for the comparator:

A1	A0	B1	B0		Y1
0	0	0	0		0
0	0	0	1		0
0	0	1	0		0
0	0	1	1		0
0	1	0	0		1
0	1	0	1		0
0	1	1	0		0
0	1	1	1		0
1	0	0	0		1
1	0	0	1		1
1	0	1	0		0
1	0	1	1		0
1	1	0	0		1
1	1	0	1		1
1	1	1	0		1
1	1	1	1		0

Available inputs: $A1, A0, B1, B0, \overline{A1}, \overline{A0}, \overline{B1}, \overline{B0}$. You cannot use Power ($V_{DD}$) and Ground ($V_{SS}$). Use the following symbols for the transmission gates.

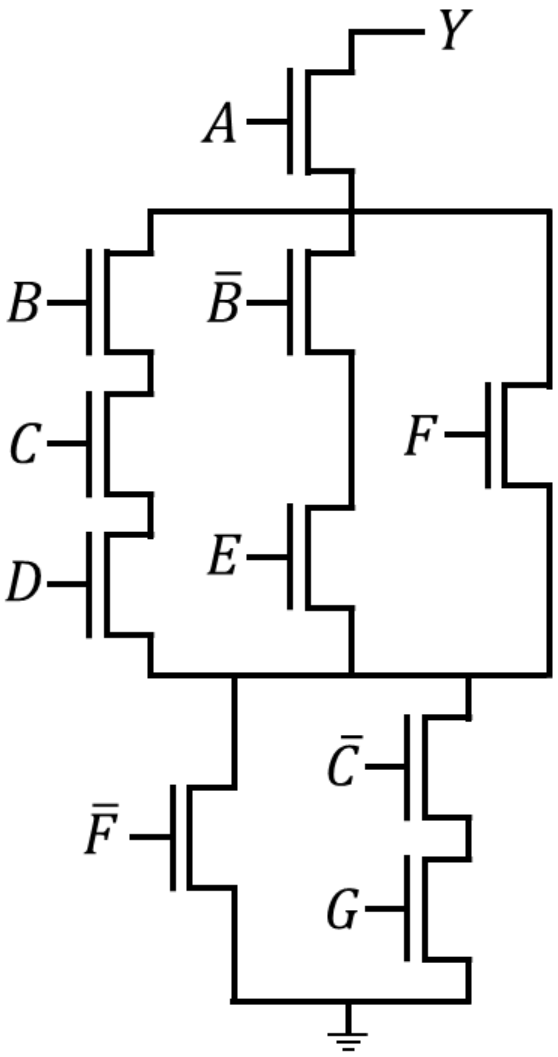


Design constraint: The total # transmission gates should be less than or equal to 12.

(# TGs≤12: 10 points. 13≤# TGs≤14: 7 points. 15≤# TGs≤16: 5 points. # TGs>16: 0 points)

Problem #4 (Transistor Sizing, 10 points)

Size the transistors in the following pull-down network. R_n is the resistance of a 1X NMOS transistor. Ignore parasitic capacitances. Target time constant: $\tau_{target} \leq R_n \cdot C_L$. Try to minimize the total area.

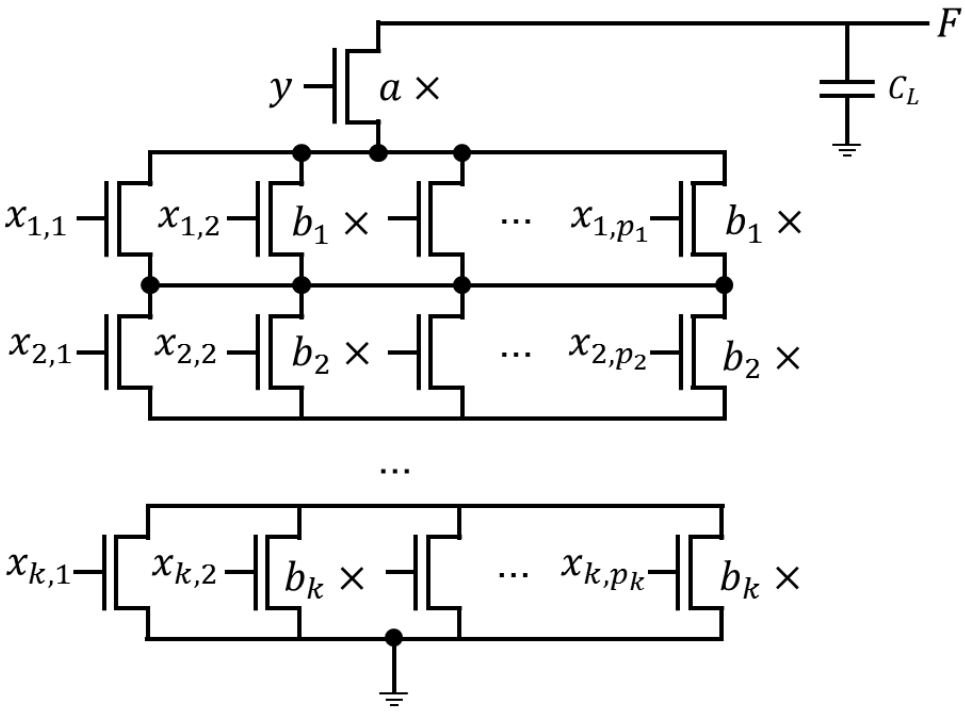


(Total width W≤48X: 10 points. W≤50X: 8 points. W≤52X: 5 points. W>52X: 3 points)

Problem #5 (Transistor Sizing, 10 points)

The following shows an NFET network of

$$F = \overline{y \cdot (x_{1,1} + \cdots + x_{1,p_1}) \cdot (x_{2,1} + \cdots + x_{2,p_2}) \cdot \ldots \cdot (x_{k,1} + \cdots + x_{k,p_k})}$$



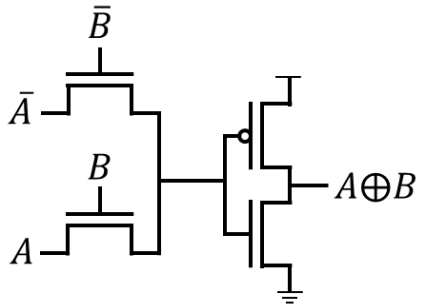
Notice that $k, p_1, \ldots, p_k$ are constants. The fall delay should be less than or equal to $R_n C_L$ where R_n is the resistance of a $1\times$ NFET. The NFET y is upsized to $a\times$ and each NFET connected to $x_{i,j}$ is upsized to $b_i\times$. We <u>minimize</u> the total width

$$W = a + b_1 \cdot p_1 + b_2 \cdot p_2 + \cdots + b_k \cdot p_k.$$

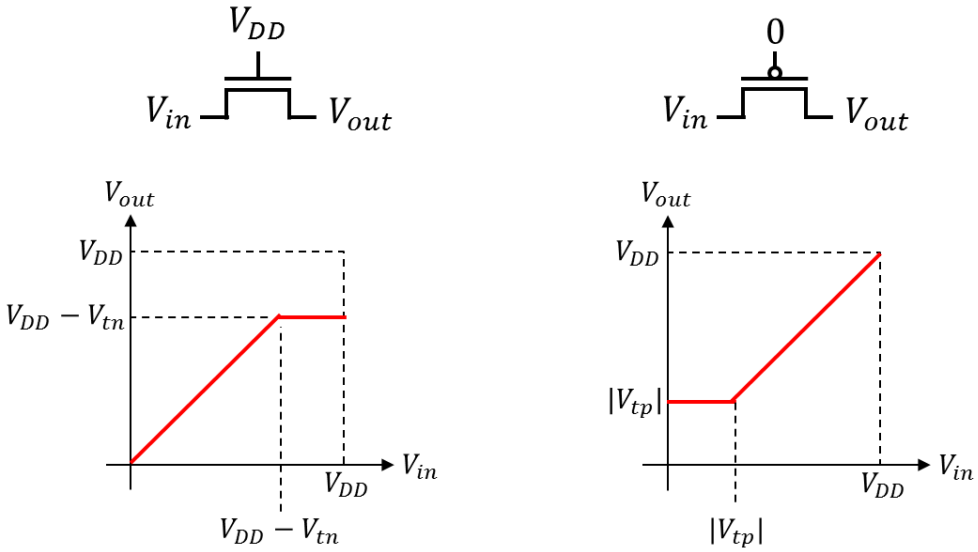
<u>Find a (the size of the NFET connected to input y) that minimizes the total width (i.e., represent a as a function of $p_1, p_2, \ldots, p_k$.</u>

Problem #6 (Pass Transistor, 10 points)

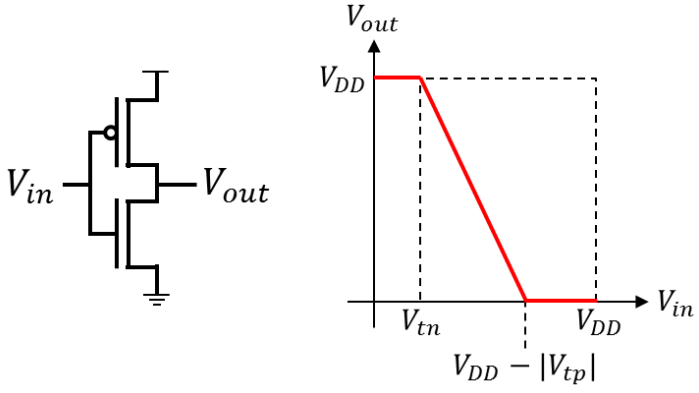
The following schematic implements an XOR gate using pass transistors.



The inverter at the output restores the signal so that the output swing can be $[0, V_{DD}]$. The following plots show the V_{DS} characteristic of the NFET when its gate voltage is V_{DD} and the V_{DS} characteristic of the PFET when its gate voltage is 0.



The following plot shows the input-output characteristic of the inverter.



V_{tn} and $|V_{tp}|$ are the threshold voltages of the NFET and the PFET, respectively. $A, B, \bar{A}, \bar{B}$ are either 0V (for 0) or V_{DD} (for 1). The swing of the final output $A \oplus B$ should be $[0, V_{DD}]$, i.e., 0V if $A \oplus B = 0$ and V_{DD} if $A \oplus B = 1$. Find all inequalities for the full output swing. (Hint: The inequalities might consist of V_{DD}, V_{tn}, and $|V_{tp}|$.)