EE434

ASIC and Digital Systems

Final Exam

May 1, 2019. (8am – 10am)

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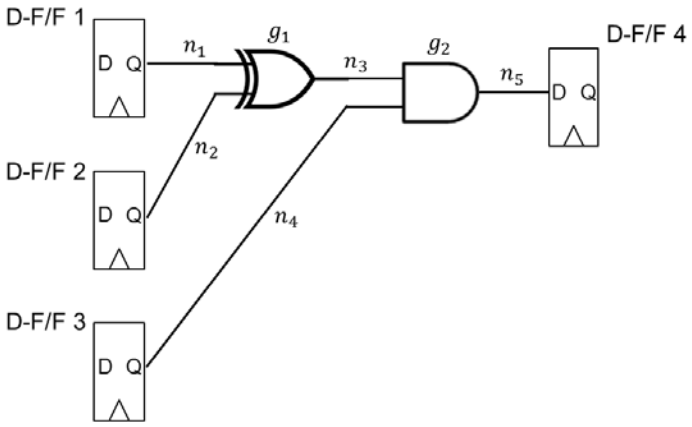
Name:

WSU ID:

Problem	Points	
1	20	
2	20	
3	30	
4	20	
5	20	
6	20	
7	20	
8	20	
Total	170	

Problem #1 (Static Timing Analysis, 20 points)

The following shows a pipeline stage. D-FF1, D-FF2, and D-FF3 are stage-k D-FFs and D-FF4 is a stage-(k+1) D-FF. n_i and g_m are net and gate delays, respectively.



The properties of D-FFp ($p = 1\sim4$) are as follows:

- Setup time: s_p (for example, s_3 is the setup time of D-FF3.)
- Hold time: h_p (for example, h_2 is the hold time of D-FF2.)
- C-Q delay: c_p (for example, c_1 is the C-Q delay of D-FF1.)
- Delay from the clock source to the clock pin of D-FFp: d_p (e.g., d_4 is the delay from the clock source to the clock pin of D-FF4.)

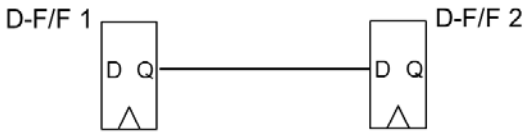
T_{CLK} is the clock period. You can also use the “MAX” and “MIN” operators.

MAX(a, b) = a (if a>b) or b (otherwise). MIN(a, b) = a (if a<b) or b (otherwise).

(1) Find all inequalities for the setup time constraints of the system shown above.

(2) Find all inequalities for the hold time constraints of the system shown above.

Problem #2 (STA & Power, 20 points)



The output Q of D-FF 1 is directly connected to the input D of D-FF 2. The length of the net is negligible, so the net delay is zero.

- T_{skew}: 0ps
- T_{h2} (the hold time of D-FF 2): 40ps
- T_{CQ1}(the clock-to-Q delay of D-FF 1): 10ps
- Available buffers: BUF_X1, BUF_X2, BUF_X4
- The input and output capacitance of a buffer: negligible (0 fF)
- The internal delay of a buffer BUF_Xs: $\frac{12}{s}$ ps (for example, the internal delay of a buffer BUF_X2 is 12/2=6ps.)
- The power consumption of a buffer BUF_Xs: $10 \cdot s + 20$ (nW) (for example, the power consumption of a BUF_X2 is 40 nW.)

You are supposed to insert buffers into the net so that you can satisfy the hold time constraint and minimize the total power consumption. Find how many buffers you should insert into the net.

Answer)

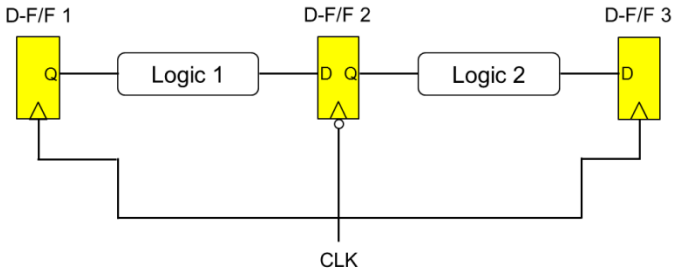
BUF_X1:

BUF_X2:

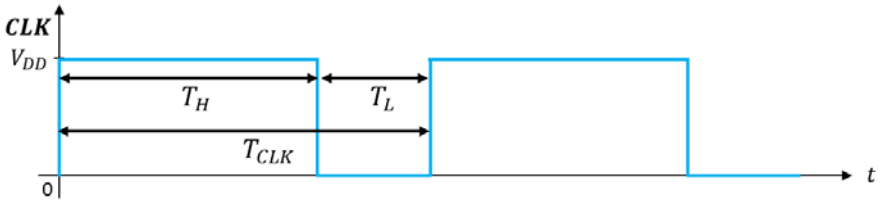
BUF_X4:

Problem #3 (STA, 30 points)

The following figure shows two pipeline stages. Notice that D-FF 1 and D-FF 3 are positive-edge-triggered FFs, whereas D-FF 2 is a negative-edge-triggered FF.



The following shows the waveform of the clock.



Notice that the duty cycle of the clock (= T_H/T_{CLK}) is not 50%.

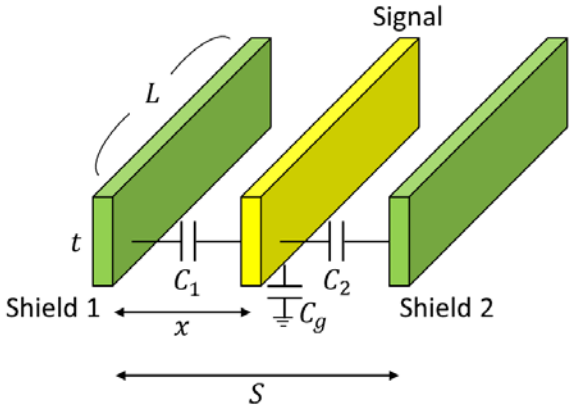
- Delay from the clock source to D-FF 1, 2, 3: d_1, d_2, d_3
- C-Q delay of D-FF 1, 2, 3: c_1, c_2, c_3
- Delay of Logic 1 and Logic 2: T_1, T_2
- Setup time of D-FF 1, 2, 3: s_1, s_2, s_3
- Hold time of D-FF 1, 2, 3: h_1, h_2, h_3

(1) Find all inequalities for the setup time constraints of the system shown above.

(2) Find all inequalities for the hold time constraints of the system shown above.

Problem #4 (Coupling, 20 points)

The following figure shows a signal net surrounded by two shield nets (Shield 1 and Shield 2) that are grounded. The coupling caps between Shield 1 and the signal net and between the signal net and Shield 2 are C_1 and C_2, respectively.

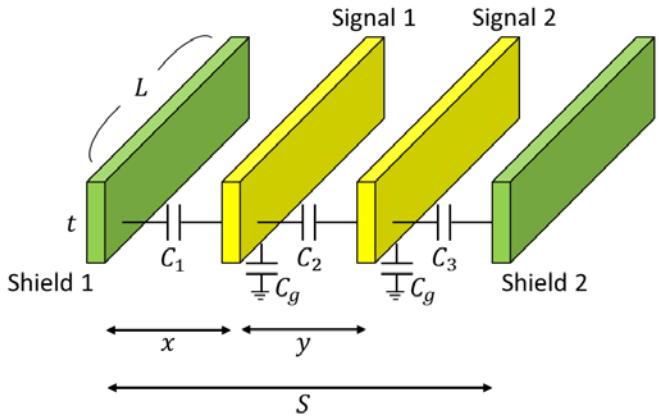


- Delay of the signal net: $(R + 0.5rL) \cdot (C_g + C_1 + C_2)$
- R (constant): The output resistance of the driver driving the signal net
- r (constant): Unit wire resistance
- L (constant): The length of the wires
- t (constant): The thickness of the wires
- S (constant): The distance between Shield 1 and Shield 2
- C_g (constant): The ground cap of the signal net
- ϵ (constant): Permittivity of the insulator material
- x (variable): The distance between Shield 1 and the signal net
- $C_1 = \frac{\epsilon tL}{x}, C_2 = \frac{\epsilon tL}{S-x}$

Find x that minimizes the delay of the signal net (you should express the optimal value of x as a function of some of the constants given above).

Problem #5 (Coupling, 20 points)

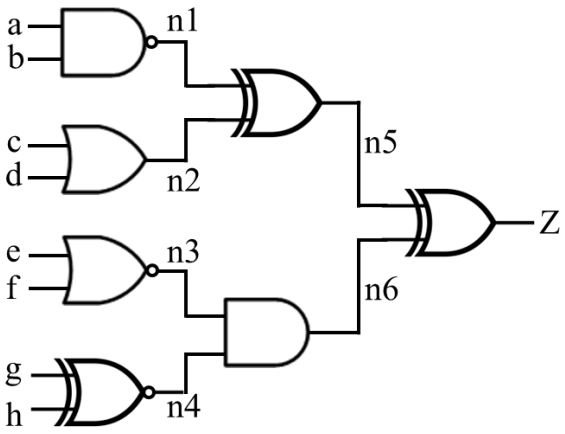
This problem is similar to Problem #4, but now we will consider two signal nets as follows.



- Delay of Signal 1: $(R + 0.5rL) \cdot (C_g + C_1 + 2C_2)$
- Delay of Signal 2: $(R + 0.5rL) \cdot (C_g + C_3 + 2C_2)$
- x (variable): The distance between Shield 1 and Signal 1
- y (variable): The distance between Signal 1 and Signal 2
- $C_1 = \frac{\epsilon tL}{x}, C_2 = \frac{\epsilon tL}{y}, C_3 = \frac{\epsilon tL}{S-(x+y)}$

Find x and y that minimize the sum of the delays of the two signal nets (you should express the optimal values of x and y as functions of some of the constants given above).

Problem #6 (Testing, 20 points)

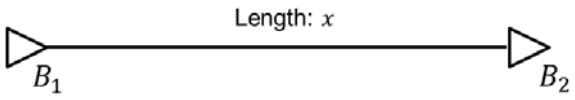


1) Find all test vectors that can detect a s-a-0 fault at input f. (You can use X for don't-cares).

2) Find all test vectors that can detect a s-a-1 fault at node $n3$. (You can use X for don't-cares).

Problem #7 (Interconnects, 20 points)

The following figure shows a buffer (B1) driving a buffer (B2). We can route the net through a lower metal layer such as metal layer 1 or an upper metal layer such as metal layer 6. The following shows the properties of the two metal layers.



	Metal layer 1	Metal layer 6
Resistivity	ρ	
Permittivity	ε	
Thickness	t	$k_1 \cdot t$
Width	w	$k_2 \cdot w$
Spacing between two metal wires	s	$k_3 \cdot s$

The wire is sufficiently long, so you can ignore the input capacitance of B2. You can also assume that the output resistance of B1 is very small (almost zero ohm).

Problem: Suppose τ_1 and τ_2 are the delays of the net routed in metal layer 1 and metal layer 6, respectively. If $k_1 = 2$, $k_2 = 4$, $k_3 = 2$, what is the ratio between τ_1 and τ_2?

Problem #8 (Interconnects, 20 points)

The following figure shows a driver (K_D), a sink (K_S), and evenly-distributed #4n buffers.

Since the buffers are evenly distributed, $s_1 = s_2 = \cdots = s_{4n+1}$ where s_j is the distance between B_j and B_{j+1} (you can think of K_D as B_0 and K_S as B_{4n+1}).

However, there is one constraint. A half of the buffers must be BUF_X1 and the other half must be BUF_X2. The following shows the characteristics of the buffers:

- BUF_X1: Output resistance (R_0), input capacitance (C_0), output capacitance (C_m), internal delay (d_0)
- BUF_X2: Output resistance ($\frac{R_0}{2}$), input capacitance ($2C_0$), output capacitance ($2C_m$), internal delay ($2d_0$)

The driver and the sink are BUF_X1 buffers.

Problem: Determine the size of each buffer (from B_1 to B_{4n}) to minimize the total delay from the driver to the sink.