# EE434

# ASIC and Digital Systems

## Midterm Exam 1

## Feb. 27, 2019. (4:10pm – 5pm)

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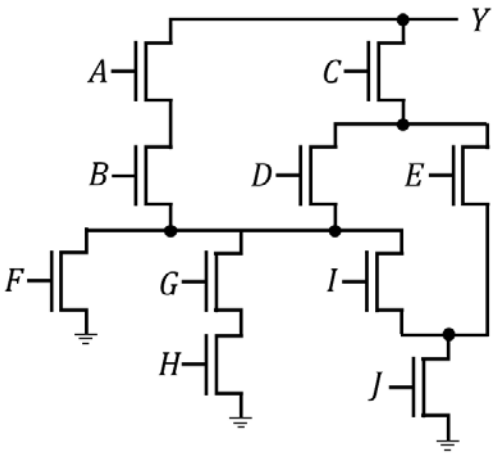
**Name:**

**WSU ID:**

| Problem | Points | |
|---|---|---|
| 1 | 10 | |
| 2 | 10 | |
| 3 | 10 | |
| 4 | 20 | |
| 5 | 20 | |
| 6 | 10 | |
| Total | 80 | |

## Problem #1 (Static CMOS gates, 10 points)

The following shows the NFET network of a static CMOS gate. Express the output $Y$ as a Boolean function of the inputs ($A$~$J$). (You don't need to simplify the expression.)



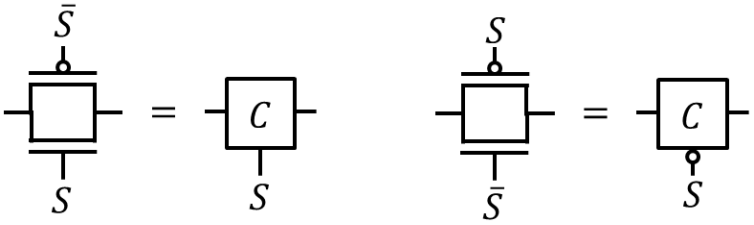

$$Y = \overline{AB(F + GH + IJ + DEJ) + CD(F + GH + IJ) + CE(J + IF + IGH)}$$

## Problem #2 (Transmission Gates, 10 points)

Design (draw a schematic) the following Boolean function using transmission gates only.

$$Y = (A \oplus B) + \overline{((A \cdot B) \oplus C)}$$

Available inputs: $A, B, C, \bar{A}, \bar{B}, \bar{C}$. You cannot use Power ($V_{DD}$) and Ground ($V_{SS}$). Use the following symbols for the transmission gates.



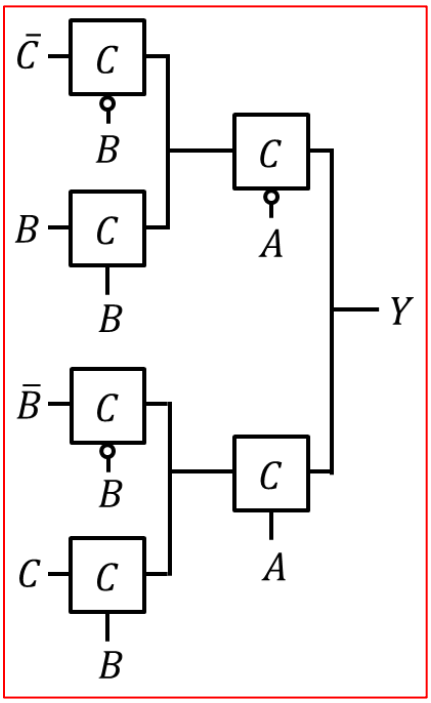

(# TGs≤6: 10 points. 7≤# TGs≤8: 7 points. 9≤# TGs≤10: 5 points. # TGs>10: 0 points)

$AB = 00: Y = \bar{C}$

$AB = 01: Y = 1$

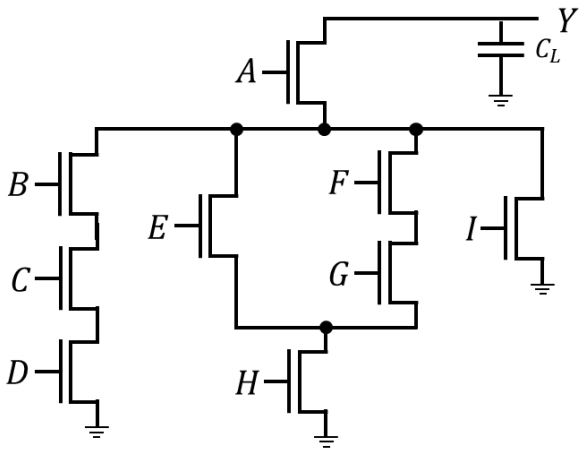
$AB = 10: Y = 1$

$AB = 11: Y = C$



## Problem #3 (Transistor Sizing, 10 points)

Size the transistors in the following pull-down network. $R_n$ is the resistance of a 1X NMOS transistor. $C_L$ is the load capacitance. Ignore parasitic capacitances. Target delay: $\tau_T \leq R_n \cdot C_L$. Try to minimize the total area.




(Total width W≤31X: 10 points. 31X<W≤32X: 8 points. 32X<W≤34X: 5 points. 34X<W: 3 points)

Longest paths: A-B-C-D, A-F-G-H, so they are upsized to 4X.

A: 4X

B: 4X

C: 4X

D: 4X

E: 2X

F: 4X

G: 4X

H: 4X

I: 4/3X

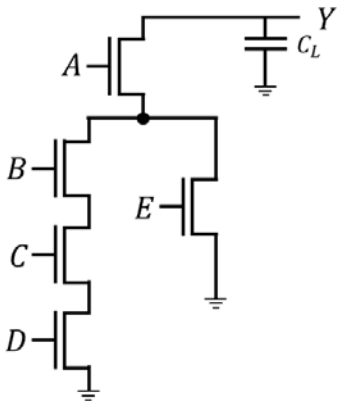
Total: 94/3X (31.33X)

Transistor A is a bottleneck, so if we upsize it to 5X, B,C,D,F,G,H can be upsized to 15/4X. In this case, E becomes 15/8X and I becomes 5/4X. The total width in this case is 245/8X, which is 30.625X.

## Problem #4 (Transistor Sizing, 20 points)

Solve either 4-(1) or 4-(2). You don't need to solve both.

(1) (20 points) Size the transistors in the following pull-down network. $R_n$ is the resistance of a 1X NMOS transistor. $C_L$ is the load capacitance. Ignore parasitic capacitances. Target delay: $\tau_T \leq R_n \cdot C_L$. *Minimize the total area (i.e., size the transistors optimally).*




A: aX, B,C,D: bX, E: cX

$$\frac{1}{a}+\frac{3}{b}=1, \frac{1}{a}+\frac{1}{c}=1$$

$$b=\frac{3a}{a-1}, c=\frac{a}{a-1}$$

$$W=a+3b+c=a+\frac{9a}{a-1}+\frac{a}{a-1}=a+10\frac{a}{a-1}$$

$$W'=1+\frac{10(a-1)-10a}{(a-1)^2}=0$$

$$a=1+\sqrt{10}, b=3+\frac{3}{\sqrt{10}}, c=1+\frac{1}{\sqrt{10}}, W=11+2\sqrt{10}$$

(2) (12 points) Answer the following questions.

(a) The optimal size of transistor A is greater than 4X (True / False).

(b) The optimal size of transistor B is greater than 4X (T / F).

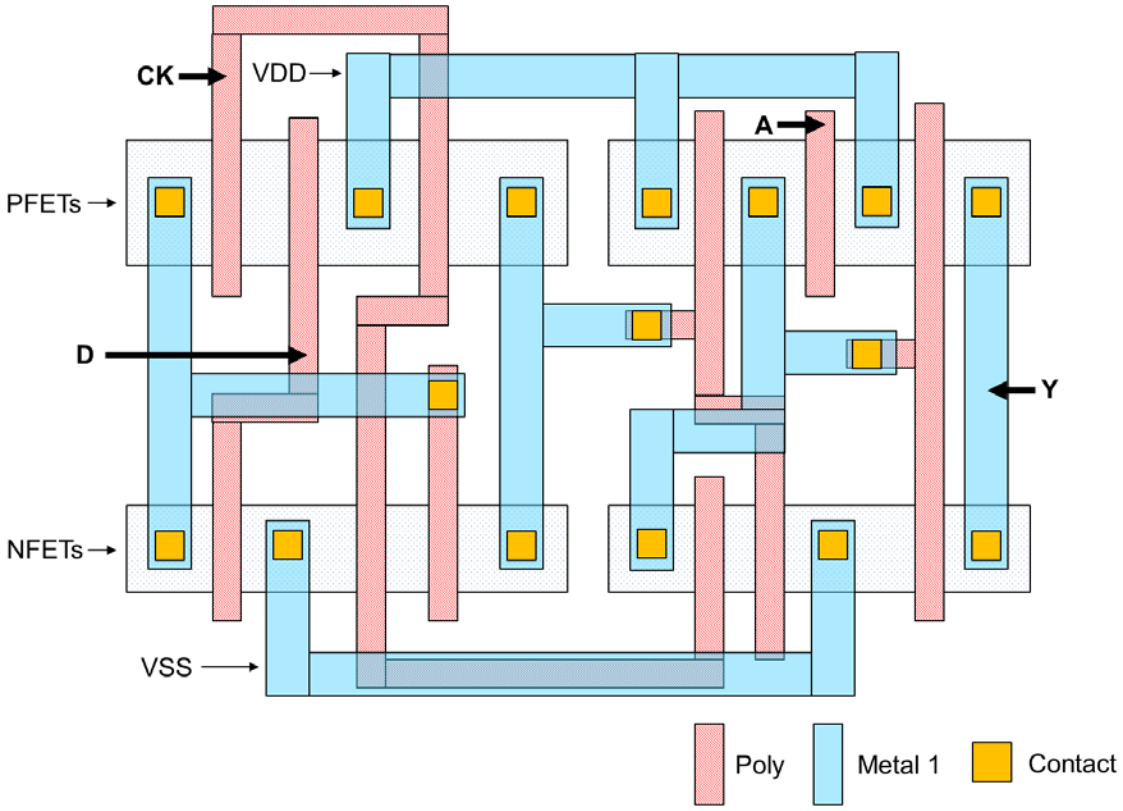
(c) The optimal size of transistor B is equal to the optimal size of transistor D (T / F).

(d) The optimal size of transistor E is greater than 2X (T / F).

(e) The optimal size of transistor C is $3 \times$ the optimal size of transistor E (T / F).

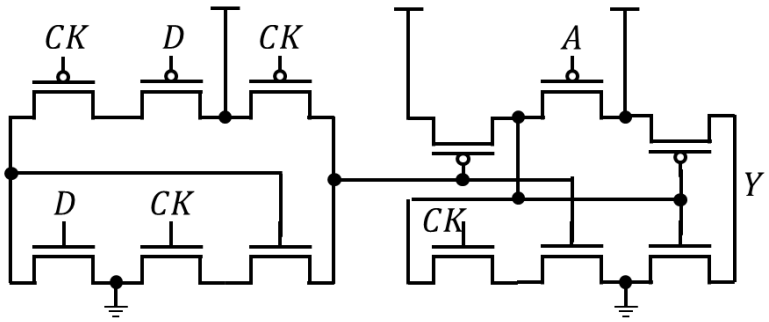
(f) The sum of the optimal widths of all the transistors is greater than or equal to 18X (T / F).

## Problem #5 (Layout, 20 points)




Signal input: A, D. Signal output: Y. Clock: CK

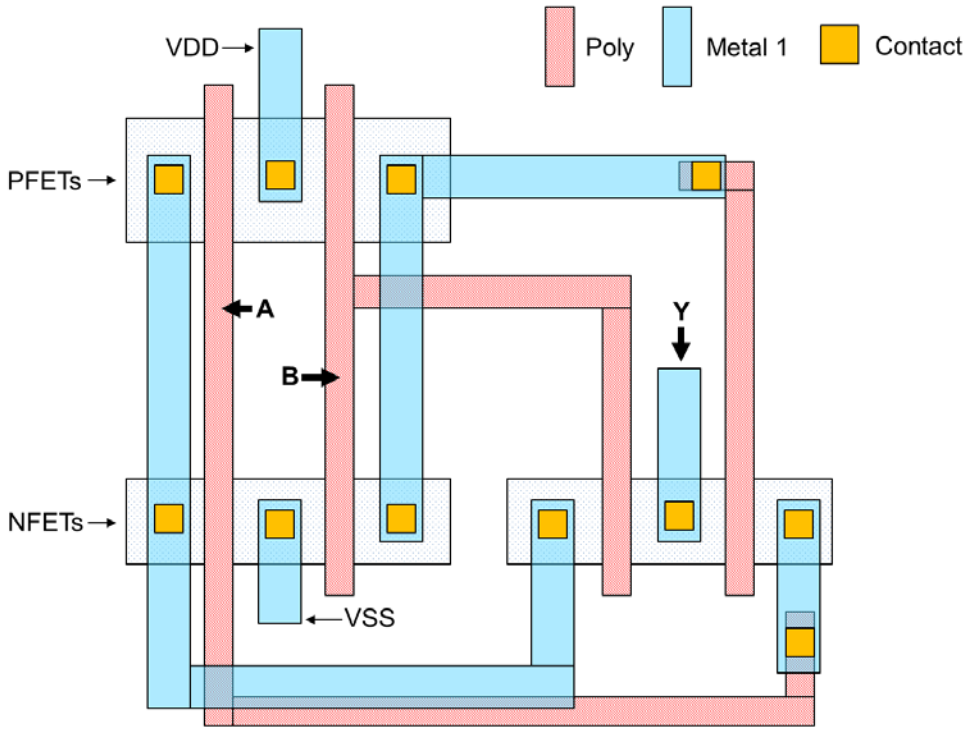
1) (10 points) Convert the layout into a transistor-level schematic.




2) (10 points) What is the function of the circuit?

This is a positive-edge-triggered D-F/F with an asynchronous active-low reset signal A.

## Problem #6 (Layout, 10 points)




Input: A, B

Output: Y

What is the function of this circuit?

It is an XOR gate. $Y = A \oplus B$.