EE434

ASIC and Digital Systems

Midterm Exam 2

Mar. 27, 2019. (4:10pm – 5pm)

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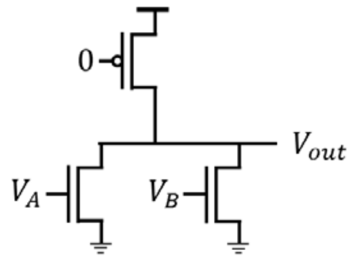
Name:

WSU ID:

Problem	Points	
1	10	
2	15	
3	20	
4	25	
5	20	
6	20	
Total	110	

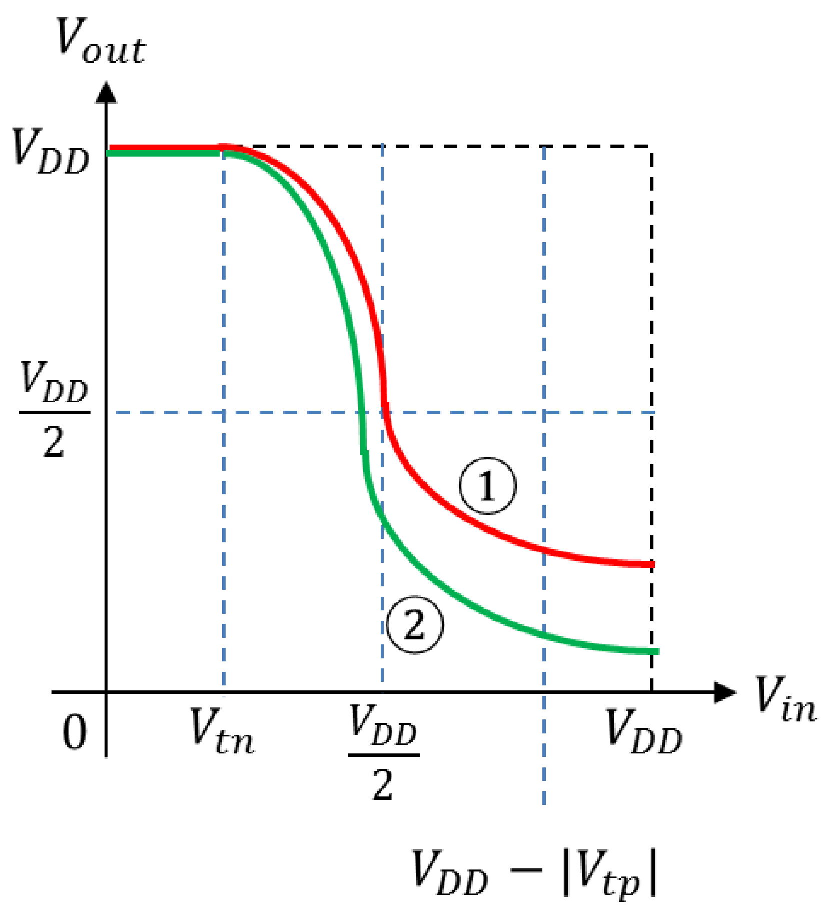
Problem #1 (DC Analysis, 10 points)

Draw a DC characteristic curve for the following pseudo-NMOS two-input NOR gate. Just a rough sketch will be accepted.



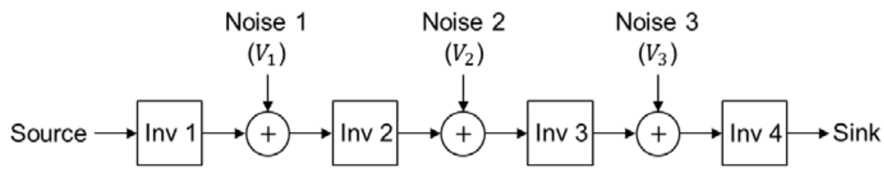
(1) For input AB: 00 → 10

(2) For input AB: 00 → 11

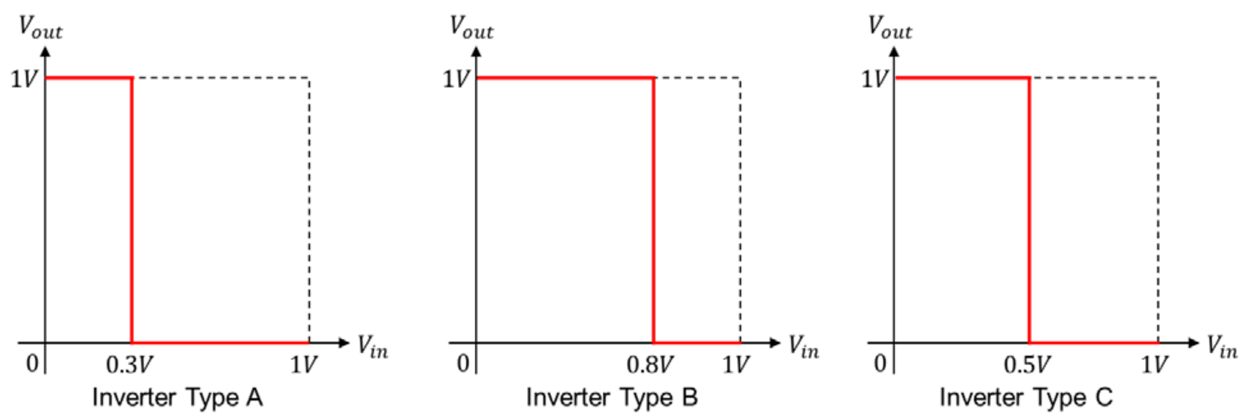


Problem #2 (DC Analysis, 15 points)

The following figure shows a chain of four inverters with three noise sources. The value at the source node is 0V (for logic 0) or 1V (for logic 1).



The following shows the DC characteristic curves for three types of inverters (Type A, B, C).



(1) (5 points) $|V_1| \leq 0.28V, |V_2| \leq 0.16V, |V_3| \leq 0.37V$. If Inv 1: Type A, Inv 2: Type B, Inv 3: Type C, Inv 4:Type C, will the inverter chain work without logic inversion at the sink node? (Yes / No)

Output: Source (0V) → Inv 1 (1V) → Noise 1 (0.72V) → Inv 2 (1V) → Noise 2 (0.84V) → Inv 3 (0V) → Noise 3 (0.37V) → Inv 4 (1V), so logic inversion occurs.

(2) (5 points) $|V_1| \leq 0.15V, |V_2| \leq 0.45V, |V_3| \leq 0.25V$. If Inv 1: Type A, Inv 2: Type B, Inv 3: Type C, Inv 4:Type A, will the inverter chain work without logic inversion at the sink node? (Yes / No)

Output: Source (0V) → Inv 1 (1V) → Noise 1 (0.85V) → Inv 2 (0V) → Noise 2 (0.45V) → Inv 3 (1V) → Noise 3 (0.75V) → Inv 4 (0V)

Source (1V) → Inv 1 (0V) → Noise 1 (0.15V) → Inv 2 (1V) → Noise 2 (0.55V) → Inv 3 (0V) → Noise 3 (0.25V) → Inv 4 (1V)

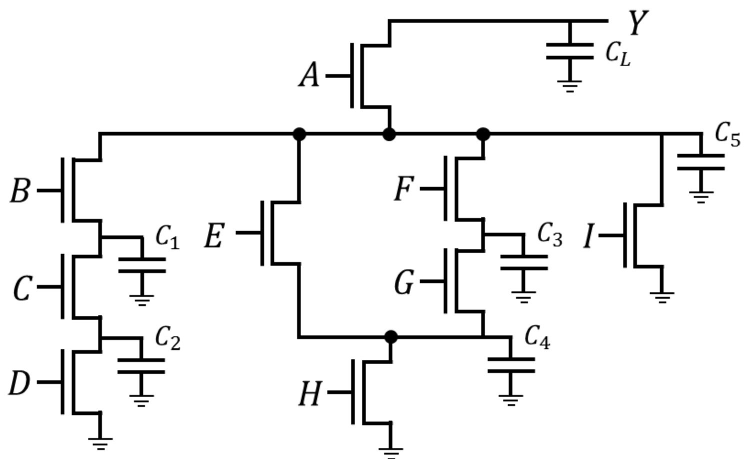
(3) (5 points) $|V_1| \leq 0.12V, |V_2| \leq 0.14V, |V_3| \leq 0.34V$. If Inv 1: Type C, Inv 2: Type A, Inv 3: Type B, Inv 4:Type A, will the inverter chain work without logic inversion at the sink node? (Yes / No)

Output: Source (0V) → Inv 1 (1V) → Noise 1 (0.88V) → Inv 2 (0V) → Noise 2 (0.14V) → Inv 3 (1V) → Noise 3 (0.66V) → Inv 4 (0V)

Source (1V) → Inv 1 (0V) → Noise 1 (0.12V) → Inv 2 (1V) → Noise 2 (0.86V) → Inv 3 (0V) → Noise 3 (0.34V) → Inv 4 (0V), so logic inversion occurs.

Problem #3 (Delay, 20 points)

Calculate the Elmore delay of the circuit shown below for the following inputs. R_n is the resistance of an NFET. C_L is the load capacitance. All the other capacitances are parasitic capacitances.



1) ABCDEFGHI = 111100000

$$\tau = R_n C_L + R_n(C_5 + C_L) + R_n(C_1 + C_5 + C_L) + R_n(C_1 + C_2 + C_5 + C_L)$$

2) ABCDEFGHI = 111010010

$$\tau = R_n C_L + R_n(C_1 + C_2 + C_5 + C_L) + R_n(C_1 + C_2 + C_4 + C_5 + C_L)$$

3) ABCDEFGHI = 101101101

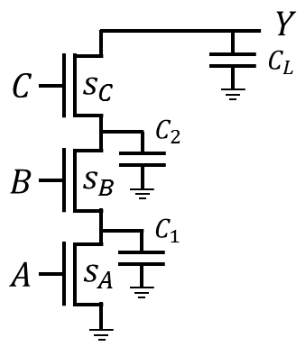
$$\tau = R_n C_L + R_n(C_3 + C_4 + C_5 + C_L)$$

4) ABCDEFGHI = 111010110

$$\tau = R_n C_L + R_n(C_1 + C_2 + C_5 + C_L) + R_n(C_1 + C_2 + C_3 + C_4 + C_5 + C_L)$$

Problem #4 (Transistor Sizing, 25 points)

The following figure shows the NFET network of a three-input NAND gate. C_L: Load capacitance. C_1, C_2: Parasitic capacitance. R_n: The resistance of a 1X NFET. Assume that C_1, C_2, C_L are independent of the widths of the NFETs. s_A, s_B, s_C: The width of NFET A, B, C, respectively. "Optimal transistor sizes" means the widths of the transistors that satisfy a given timing constraint and minimize the sum of the widths.



(1) (7 points) Express the Elmore delay of the NAND gate as a function of $R_n, s_A, s_B, s_C, C_1, C_2, C_L$.

$$\tau = \frac{R_n}{s_C} C_L + \frac{R_n}{s_B}(C_2 + C_L) + \frac{R_n}{s_A}(C_1 + C_2 + C_L)$$

(2) (18 points) Answer the following questions.

(a) If C_1 increases, we should increase the width of transistor A for optimal transistor sizing (True / False).

(b) If C_1 increases, we should increase the width of transistor B for optimal transistor sizing (True / False).

(c) If C_1 increases, we should increase the width of transistor C for optimal transistor sizing (True / False).

(d) If C_2 increases, we should increase the width of transistor A for optimal transistor sizing (True / False).

(e) If C_2 increases, we should increase the width of transistor B for optimal transistor sizing (True / False).

(f) If C_2 increases, we should increase the width of transistor C for optimal transistor sizing (True / False).

(g) If C_L increases, we should increase the width of transistor A for optimal transistor sizing (True / False).

(h) If C_L increases, we should increase the width of transistor B for optimal transistor sizing (True / False).

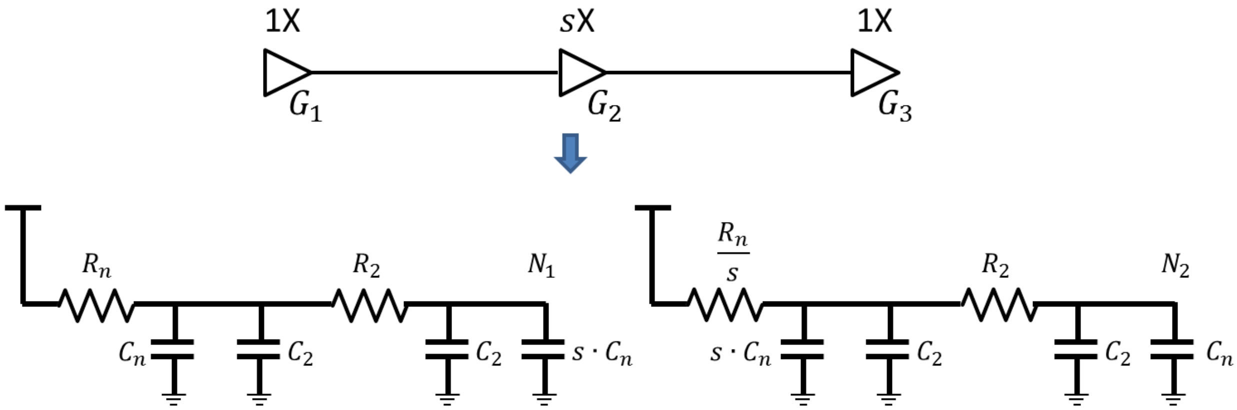
(i) If C_L increases, we should increase the width of transistor C for optimal transistor sizing (True / False).

We can answer the above questions by deeply investigating the Elmore delay equation. However, we can also optimally get the result as follows.

Minimize $s_A + s_B + s_C$. Let $x_i = 1/s_i$. Then, minimize $W = \frac{1}{x_A} + \frac{1}{x_B} + \frac{1}{x_C}$ for $\tau = R_n C_L x_C + R_n(C_2 + C_L)x_B + R_n(C_1 + C_2 + C_L)x_A = t$ where t is a given delay constraint. Assuming x_A and x_B are two independent variables, $\frac{\partial \tau}{\partial x_A} = R_n(C_1 + C_2 + C_L) + R_n C_L \frac{\partial x_C}{\partial x_A} = 0$, $\frac{\partial \tau}{\partial x_B} = R_n(C_2 + C_L) + R_n C_L \frac{\partial x_C}{\partial x_B} = 0$. Now, $\frac{\partial W}{\partial x_A} = -\frac{1}{x_A{}^2} - \frac{1}{x_C{}^2} \cdot \frac{\partial x_C}{\partial x_A} = 0$, $\frac{\partial W}{\partial x_B} = -\frac{1}{x_B{}^2} - \frac{1}{x_C{}^2} \cdot \frac{\partial x_C}{\partial x_B} = 0$. Thus, $x_C = x_A\sqrt{\frac{C_1+C_2+C_L}{C_L}}$, $x_C = x_B\sqrt{\frac{C_2+C_L}{C_L}}$. Thus, $R_n C_L x_C + R_n(C_2 + C_L)x_C\sqrt{\frac{C_L}{C_2+C_L}} + R_n(C_1 + C_2 + C_L)x_C\sqrt{\frac{C_L}{C_1+C_2+C_L}} = t$, so $x_C = \frac{t}{R_n(C_L+\sqrt{C_L(C_2+C_L)}+\sqrt{C_L(C_1+C_2+C_L)})}$. $x_A = \frac{t}{R_n((C_1+C_2+C_L)+\sqrt{(C_2+C_L)(C_1+C_2+C_L)}+\sqrt{C_L(C_1+C_2+C_L)})}$. $x_B = \frac{t}{R_n((C_2+C_L)+\sqrt{(C_2+C_L)(C_1+C_2+C_L)}+\sqrt{C_L(C_2+C_L)})}$.

Thus, $s_A = \frac{1}{t} \cdot R_n \cdot \left[(C_1 + C_2 + C_L) + \sqrt{(C_2 + C_L)(C_1 + C_2 + C_L)} + \sqrt{C_L(C_1 + C_2 + C_L)}\right]$, $s_B = \frac{1}{t} \cdot R_n \cdot \left[(C_2 + C_L) + \sqrt{(C_2 + C_L)(C_1 + C_2 + C_L)} + \sqrt{C_L(C_2 + C_L)}\right]$, $s_C = \frac{1}{t} \cdot R_n \cdot \left[C_L + \sqrt{C_L(C_2 + C_L)} + \sqrt{C_L(C_1 + C_2 + C_L)}\right]$.

Problem #5 (Interconnect, 20 points)



The figure shown above simulates the delay of the signal path from gate G_1 to gate G_3. For the delay calculation, we use the two RC trees. The left-hand one is for the first half (from G_1 to G_2) of the path and the right-hand one is for the second half (from G_2 to G_3). The total delay is estimated by the sum of the delays at node N_1 and N_2.

- G_1 and G_3 are 1X cells, so their output resistances, output capacitances, and input capacitances are R_n, C_n, and C_n, respectively.
- G_2 is upsized to sX, so its output resistance, output capacitance, and input capacitance are $\frac{R_n}{s}$, sC_n, and sC_n, respectively.
- R_2 and C_2 model the wires.
- R_n, C_n, C_2, R_2 are constants. s is the only variable in this problem.

(1) (7 points) Express the total delay as a function of s, R_n, C_n, R_2, and C_2.

$$\tau = R_2(C_2 + sC_n) + R_n(C_n + 2C_2 + sC_n) + R_2(C_2 + C_n) + \frac{R_n}{s}(sC_n + 2C_2 + C_n)$$

(2) (5 points) Express optimal s minimizing the total delay as a function of R_n, C_n, R_2, and C_2.

$\frac{d\tau}{ds} = R_2C_n + R_nC_n - \frac{R_n(2C_2+C_n)}{s^2} = 0$, so $s = \sqrt{\frac{R_n(2C_2+C_n)}{C_n(R_2+R_n)}} = \sqrt{\frac{1+2\frac{C_2}{C_n}}{1+\frac{R_2}{R_n}}}$

(3) (8 points) Answer the following questions.

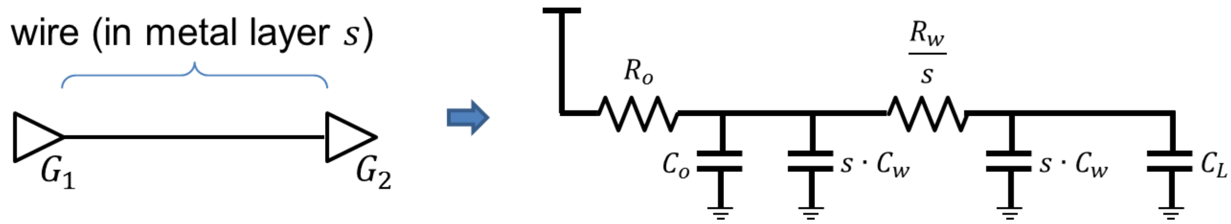
(a) If R_n increases, we should increase s for minimum delay. (True / False)

(b) If C_n increases, we should increase s for minimum delay. (True / False)

(c) If R_2 increases, we should increase s for minimum delay. (True / False)

(d) If C_2 increases, we should increase s for minimum delay. (True / False)

Problem #6 (Interconnect, 20 points)



The figure shown above simulates the delay of a net routed in metal layer s.

- R_o, C_o: Output resistance and capacitance of G_1, respectively (constants).
- C_L: Load capacitance (constant)
- R_w, C_w: Resistance and capacitance of the wire, respectively (constants).
- s: Metal layer (variable)

When we route the net in a layout, we can use any metal layer. If we select an upper layer (e.g., Metal layer 10) for the routing of the net, the resistance of the wire goes down, but the capacitance of the wire goes up. Similarly, if we select a lower layer (e.g., Metal layer 3), the resistance of the wire goes up, but the capacitance of the wire goes down. The RC tree provides a very simple model for the delay estimation.

(1) (5 points) Express the delay from G_1 to G_2 as a function of R_o, C_o, R_w, C_w, C_L, and s.

$$\tau = \frac{R_w}{s} \cdot (s \cdot C_w + C_L) + R_o(C_o + 2sC_w + C_L) = (R_w C_w + R_o C_o + R_o C_L) + 2R_o C_w s + \frac{R_w C_L}{s}$$

(2) (5 points) Find s minimizing the delay (express s as a function of R_o, C_o, R_w, C_w, and C_L.

$$\frac{d\tau}{ds} = 2R_o C_w - \frac{R_w C_L}{s^2} = 0, \text{ so } s = \sqrt{\frac{R_w C_L}{2R_o C_w}}$$

(3) (8 points) Answer the following questions.

(a) If R_w increases, we should increase s to minimize the delay. (True / False)

(b) If R_o increases, we should increase s to minimize the delay. (True / False)

(c) If C_w increases, we should increase s to minimize the delay. (True / False)

(d) If C_o increases, we should increase s to minimize the delay. (True / False)

(e) If C_L increases, we should increase s to minimize the delay. (True / False)