EE434

ASIC and Digital Systems

Final Exam

May 5, 2020. (8am – 10am)

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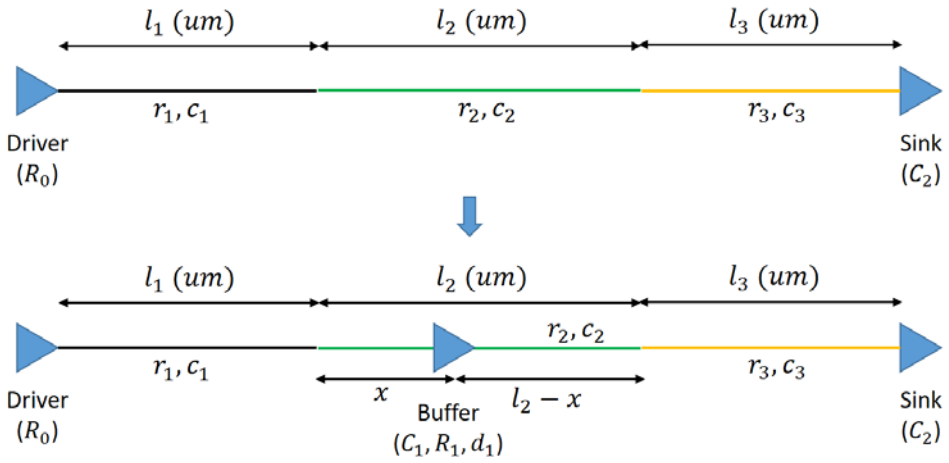
Name:

WSU ID:

Problem	Points	
1	30	
2	40	
3	30	
4	50	
5	20	
6	50	
7	40	
Total	260	

Problem #1 (Interconnects, 30 points)



The figure shows a net composed of three wire segments. The length and unit wire R and C of section k $(k = 1, 2, 3)$ are l_k, r_k, and c_k, respectively as shown in the figure. The output resistance of the driver is R_0, the input capacitance of the sink is C_2, and the output resistance, input capacitance, and the delay of a buffer is R_1, C_1, and d_1, respectively. We are going to insert a buffer into the second section. The first and third sections are not bufferable.

(1) Find the optimal location for the buffer insertion (express the location as a function of the constants). (10 points)

Let's assume that the distance from the left side of the second section to the buffer is $x\ (um)$ (so, $0 \le x \le l_2$). Then, the delay of the left side of the buffer is

$$\tau_1 = R_0(c_1 l_1 + c_2 x + C_1) + r_1 l_1 (c_2 x + C_1) + \frac{1}{2} r_1 c_1 {l_1}^2 + r_2 x C_1 + \frac{1}{2} r_2 c_2 x^2$$

The delay of the right side is

$$\tau_2 = R_1(c_2(l_2 - x) + c_3 l_3 + C_2) + r_2(l_2 - x)(c_3 l_3 + C_2) + \frac{1}{2} r_2 c_2 (l_2 - x)^2 + r_3 l_3 C_2 + \frac{1}{2} r_3 c_3 {l_3}^2$$

and the total delay is

$$\tau = \tau_1 + d_1 + \tau_2$$

$$\frac{d\tau}{dx} = R_0 c_2 + r_1 l_1 c_2 + r_2 C_1 + r_2 c_2 x - R_1 c_2 - r_2(c_3 l_3 + C_2) - r_2 c_2 (l_2 - x) = 0$$

$$x(2 r_2 c_2) = (R_1 - R_0) c_2 + (C_2 - C_1) r_2 - r_1 c_2 l_1 + r_2 c_3 l_3 + r_2 c_2 l_2$$

$$\therefore x = \frac{1}{2}\left\{\frac{R_1 - R_0}{r_2} + \frac{C_2 - C_1}{c_2} - \frac{r_1}{r_2} l_1 + l_2 + \frac{c_3}{c_2} l_3\right\}$$

(2) Answer the following questions. (Correct: +2 points. Wrong: -1 point. No answer: 0.)

(1) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x = \frac{1}{2} l_2$. (**True** / False)

(2) If $R_0 < R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / **False**)

(3) If $R_0 = R_1$, $C_1 < C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / **False**)

(4) If $R_0 = R_1$, $C_1 = C_2$, $r_1 < r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / **False**)

(5) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 > r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / **False**)

(6) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 < c_2 = c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / **False**)

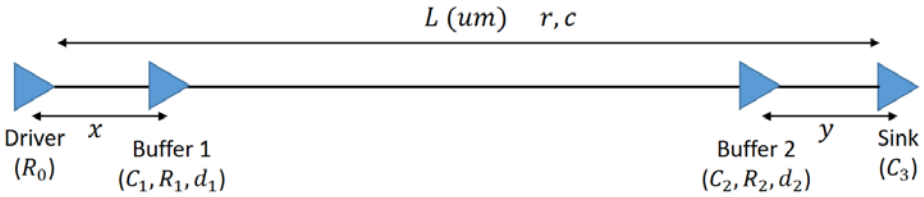
(7) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 > c_3$, and $l_1 = l_2 = l_3$, then $x < \frac{1}{2} l_2$. (**True** / False)

(8) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 < l_2 = l_3$, then $x < \frac{1}{2} l_2$. (True / **False**)

(9) If $R_0 = R_1$, $C_1 = C_2$, $r_1 = r_2 = r_3$, $c_1 = c_2 = c_3$, and $l_1 = l_2 > l_3$, then $x < \frac{1}{2} l_2$. (**True** / False)

(10) If r_3 increases, x increases (i.e., the optimal buffer location is shifted to the right.) (True / **False**)

Problem #2 (Interconnects, 40 points)



The figure shows a net composed of a long wire whose unit resistance and capacitance are r and c, respectively. We want to insert two buffers, Buffer 1 and Buffer 2 ($0 \le x$, $0 \le y$, $x + y \le L$). The output resistance ($R_{\#}$), input capacitance ($C_{\#}$), and internal delay ($d_{\#}$) of each cell are shown above.

(a) Find the optimal locations for Buffer 1 and Buffer 2 (express x (and also y) as a function of the constants). Hint: Express the total delay as a function of x and y. Then, different it w.r.t. x and set it to zero. Differentiate it w.r.t. y and set it to zero. Then, you get two equations for two variables, x and y. Solve it. (12 points)

$$\tau_1 = R_0(C_1 + cx) + rxC_1 + \frac{1}{2}rcx^2$$

$$\tau_2 = R_1\{C_2 + c(L - x - y)\} + r(L - x - y)C_2 + \frac{1}{2}rc(L - x - y)^2$$

$$\tau_3 = R_2(C_3 + cy) + ryC_3 + \frac{1}{2}rcy^2$$

Total delay $\tau = \tau_1 + d_1 + \tau_2 + d_2 + \tau_3$

$$\frac{\partial \tau}{\partial x} = R_0c + rC_1 + rcx - R_1c - rC_2 - rc(L - x - y) = 0$$

$$\frac{\partial \tau}{\partial y} = R_2c + rC_3 + rcy - R_1c - rC_2 - rc(L - x - y) = 0$$

$$2rcx + rcy = rcL + (R_1 - R_0)c + (C_2 - C_1)r$$

$$rcx + 2rcy = rcL + (R_1 - R_2)c + (C_2 - C_3)r$$

$$\therefore x = \frac{1}{3}\left\{L + \frac{R_1 + R_2 - 2R_0}{r} + \frac{C_2 + C_3 - 2C_1}{c}\right\}$$

$$y = \frac{1}{3}\left\{L + \frac{R_0 + R_1 - 2R_2}{r} + \frac{C_1 + C_2 - 2C_3}{c}\right\}$$

(b) Answer the following questions. (Correct: +2 points. Wrong: -1 point. No answer: 0.)

Notice that if x increases, Buffer 1 is shifted to the right.

However, if y increases, Buffer 2 is shifted to the left.

(1) If $R_0 = R_1 = R_2$ and $C_1 = C_2 = C_3$, then $x = \frac{1}{3}L$. (**True** / False)

(2) If $R_0 = R_1 = R_2$ and $C_1 = C_2 = C_3$, then $y = \frac{1}{3}L$. (**True** / False)

(3) If R_0 increases, x increases. (True / **False**)

(4) If R_0 increases, y increases. (**True** / False)

(5) If R_1 increases, x increases. (**True** / False)

(6) If R_1 increases, y increases. (**True** / False)

(7) If R_2 increases, x increases. (**True** / False)

(8) If R_2 increases, y increases. (True / **False**)

(9) If C_1 increases, x increases. (True / **False**)

(10) If C_1 increases, y increases. (**True** / False)

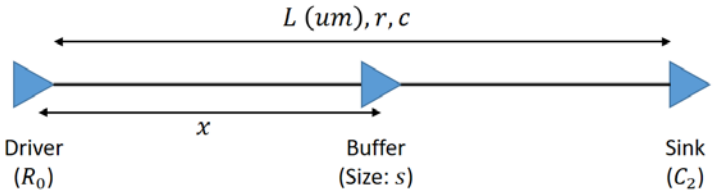
(11) If C_2 increases, x increases. (**True** / False)

(12) If C_2 increases, y increases. (**True** / False)

(13) If C_3 increases, x increases. (**True** / False)

(14) If C_3 increases, y increases. (True / **False**)

Problem #3 (Interconnects, 30 points)



The figure shows a long wire whose length, unit resistance and capacitance are L, r, and c, respectively. We want to insert a buffer ($0 \le x \le L$). The size of the buffer is s and its output resistance, input capacitance, and internal delay are as follows:

- Output resistance: $\frac{R}{s}$ (where R is a constant)
- Input capacitance: sP (where P is a constant)
- Internal delay: sD (where D is a constant)

Notice that there are two variables, x and s.

(a) Express the total delay as a function of the variables and the constants. (7 points)

$$\tau = R_0(cx + sP) + rx(sP) + \frac{1}{2}rcx^2 + sD + \frac{R}{s}\{c(L-x) + C_2\} + r(L-x)C_2 + \frac{1}{2}rc(L-x)^2$$

(b) Assuming the location (x) is given (i.e., you can treat it as a constant.), find the optimal size (s) of the buffer, .i.e., express the optimal value of s as a function of the constants and x. (7 points)

$$\frac{\partial \tau}{\partial s} = R_0 P + rxP + D - \frac{R\{c(L-x) + C_2\}}{s^2} = 0$$

$$s = \sqrt{\frac{R\{c(L-x) + C_2\}}{(R_0 + rx)P + D}}$$

(c) Answer the following questions. (Correct: +2 points. Wrong: -1 point. No answer: 0.)

(1) If x increases, s increases. (True / **False**)

(2) If R increases, s increases. (**True** / False)

(3) If c increases, s increases. (**True** / False)

(4) If C_2 increases, s increases. (**True** / False)

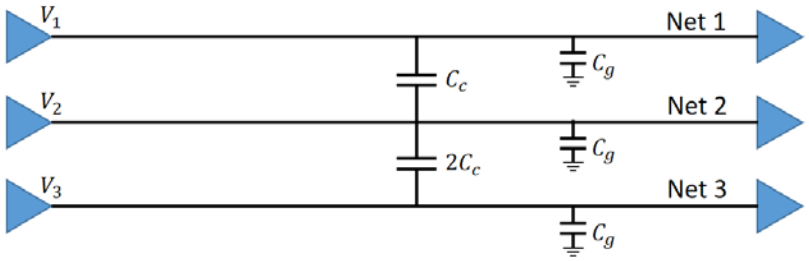
(5) If R_0 increases, s increases. (True / **False**)

(6) If r increases, s increases. (True / **False**)

(7) If P increases, s increases. (True / **False**)

(8) If D increases, s increases. (True / **False**)

Problem #4 (Coupling, 50 points)



The figure shows three parallel nets. The coupling capacitance between Net 1 and Net 2 is C_C. The coupling capacitance between Net 2 and Net 3 is $2C_C$. The following shows a three-bit binary encoding technique for four decimal numbers (0, 1, 2, 3).

Value	Encoding
0	000
1	010
2	101
3	111

(1) Calculate the total effective capacitance of Net 1 for all possible transitions (0→1, 0→2, 0→3, 1→0, 1→2, 1→3, 2→0, 2→1, 2→3, 3→0, 3→1, 3→2) for the encoding technique, i.e., calculate the sum of the effective capacitances of Net 1 for all possible transitions. (10 points)

0→1: 0, 0→2: $C_g + C_c$, 0→3: C_g, 1→0: 0, 1→2: $C_g + 2C_c$, 1→3: $C_g + C_c$, 2→0: $C_g + C_c$, 2→1: $C_g + 2C_c$, 2→3: 0, 3→0: C_g, 3→1: $C_g + C_c$, 3→2: 0. (Notice that a→b and b→a have the same effective capacitance.)

Total effective capacitance: $8C_g + 8C_c$

(2) Repeat it for Net 2. (10 points)

0→1: $C_g + 3C_c$, 0→2: 0, 0→3: C_g, 1→2: $C_g + 6C_c$, 1→3: 0, 2→3: $C_g + 3C_c$.

Total effective capacitance: $8C_g + 24C_c$

(3) Repeat it for Net 3. (10 points)

0→1: 0, 0→2: $C_g + C_c$, 0→3: C_g, 1→2: $C_g + 4C_c$, 1→3: $C_g + 2C_c$, 2→3: 0

Total effective capacitance: $8C_g + 14C_c$

Thus, the total effective capacitance for all the nets for all the possible transitions is $24C_g + 46C_c$

(4) Find a new three-bit encoding of the four values (0, 1, 2, 3) that minimizes the total effective capacitance of the three nets for all possible transitions (Assume $C_g = C_c$). (20 points)

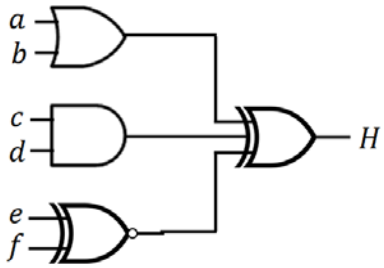
Value	Encoding
0	000
1	100
2	110
3	111

In this case,
0→1: $C_g + C_c\ (Net\ 1) + 0\ (Net\ 2) + 0\ (Net\ 3) = C_g + C_c$
0→2: $C_g\ (Net\ 1) + C_g + 2C_c\ (Net\ 2) + 0\ (Net\ 3) = 2C_g + 2C_c$
0→3: $C_g\ (Net\ 1) + C_g\ (Net\ 2) + C_g\ (Net\ 3) = 3C_g$
1→2: $0\ (Net\ 1) + C_g + 3C_c\ (Net\ 2) + 0\ (Net\ 3) = C_g + 3C_c$
1→3: $0\ (Net\ 1) + C_g + C_c\ (Net\ 2) + C_g\ (Net\ 3) = 2C_g + C_c$
2→3: $0\ (Net\ 1) + 0\ (Net\ 2) + C_g + 2C_c\ (Net\ 3) = C_g + 2C_c$

Total effective capacitance (for Net 1, 2, and 3): $20C_g + 18C_c = 38C_g$

Problem #5 (Testing, 20 points)

The following shows $H = (a + b) \oplus (c \cdot d) \oplus (\overline{e \oplus f})$. Answer the following questions.



(1) Find all input vectors that can detect a s-a-0 fault at input a. (10 points)

$$H \oplus H_f = \{(a + b) \oplus (c \cdot d) \oplus (\overline{e \oplus f})\} \oplus \{(b) \oplus (c \cdot d) \oplus (\overline{e \oplus f})\} = 1$$

Thus, a should be 1. Then,

$$H(a = 1) \oplus H_f = \{1 \oplus (c \cdot d) \oplus (\overline{e \oplus f})\} \oplus \{(b) \oplus (c \cdot d) \oplus (\overline{e \oplus f})\} = 1$$

Thus, b should be 0. Then,

$$H(ab = 10) \oplus H_f = \{1 \oplus (c \cdot d) \oplus (\overline{e \oplus f})\} \oplus \{(c \cdot d) \oplus (\overline{e \oplus f})\} = 1$$

Now, it is always true regardless of c, d, e, f.

Answer: $(abcdef) = (10XXXX)$ (where X is a don't care).

(2) Find all input vectors that can detect a s-a-1 fault at input e. (10 points)

$$H \oplus H_f = \{(a + b) \oplus (c \cdot d) \oplus (\overline{e \oplus f})\} \oplus \{(a + b) \oplus (c \cdot d) \oplus (\overline{1 \oplus f})\} = 1$$

$$H \oplus H_f = \{(a + b) \oplus (c \cdot d) \oplus (\overline{e \oplus f})\} \oplus \{(a + b) \oplus (c \cdot d) \oplus f\} = 1$$

Thus, e should be 0. Then,

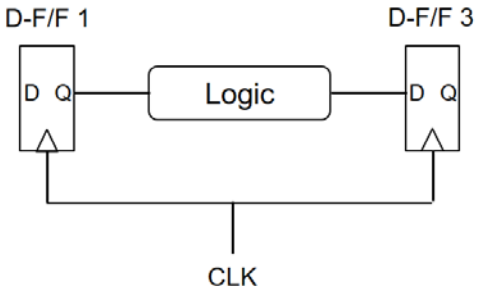
$$H(e = 0) \oplus H_f = \{(a + b) \oplus (c \cdot d) \oplus (\bar{f})\} \oplus \{(a + b) \oplus (c \cdot d) \oplus f\} = 1$$

Now, this is always true for any (a, b, c, d, f).

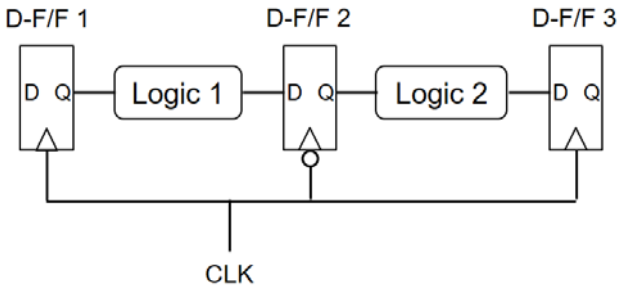
Answer: $(abcdef) = (XXXX0X)$

Problem #6 (Static Timing Analysis, 50 points)

The following shows two pipelining methodologies. Figure (a) shows a logic in a single pipeline stage. Figure (b) shows a partitioned version in which two pipeline stages are cascaded and the flip-flop in the middle is negative-edge-triggered.



(a)



(b)

Parameters

- d_1, d_2, d_3: The delay from the clock source to Flip-Flop 1, 2, 3
- c_1, c_2, c_3: Clock-to-Q delay (T_{CQ}) of Flip-Flop 1, 2, 3
- s_1, s_2, s_3: Setup time of Flip-Flop 1, 2, 3
- T_A, T_B : Clock period for Figure (a) and (b)
- N ($\gg 1$): # instructions to execute
- T_L: The logic delay in Figure (a). In Figure (b), the delay of each logic is $\frac{T_L}{2}$.
- Execution time of the system in Figure (a): $(N+1) \cdot T_A$
- Execution time of the system in Figure (b): $(N+3) \cdot T_B$

For the clock periods, we use the minimum clock periods that satisfy all the setup time constraints. Notice that the clock duty cycle is 50%.

(1) The system in Figure (a) has one setup time constraint. Show the inequality. (10 points)

$$d_1 + c_1 + T_L \leq d_3 + T_A - s_3$$

(2) The system in Figure (b) has two setup time constraints. Show the inequalities. (16 points)

$$d_1 + c_1 + \frac{T_L}{2} \leq d_2 + \frac{T_B}{2} - s_2$$

$$d_2 + \frac{T_B}{2} + c_2 + \frac{T_L}{2} \leq d_3 + T_B - s_3$$

(3) Now, you have execution times for Figure (a) and (b). Answer the following questions. (24 points)

For Figure (a), $T_A = d_1 + c_1 + T_L - d_3 + s_3$

For Figure (b), $T_B = d_1 - d_3 + c_1 + c_2 + T_L + s_2 + s_3$

(a) For Figure (a): If d_1 increases, the execution time increases (**True** / False).

(b) For Figure (a): If c_1 increases, the execution time increases (**True** / False).

(c) For Figure (a): If T_L increases, the execution time increases (**True** / False).

(d) For Figure (a): If d_3 increases, the execution time increases (True / **False**).

(e) For Figure (a): If s_3 increases, the execution time increases (**True** / False).

(f) For Figure (b): If d_1 increases, the execution time increases (**True** / False).

(g) For Figure (b): If c_1 increases, the execution time increases (**True** / False).

(h) For Figure (b): If T_L increases, the execution time increases (**True** / False).

(i) For Figure (b): If d_3 increases, the execution time increases (True / **False**).

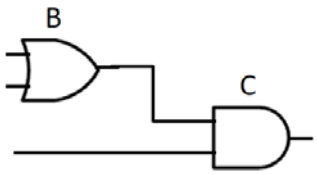
(j) For Figure (b): If s_2 increases, the execution time increases (**True** / False).

(k) For Figure (b): If s_3 increases, the execution time increases (**True** / False).

(l) For Figure (b): If c_2 increases, the execution time increases (**True** / False).

Problem #7 (Static Timing Analysis, 40 points)

The following shows two gates B and C, which are in the middle of a circuit.



"A gate has a (setup or hold) time violation" means that at least one of the paths going through the gate violates given (setup or hold) time constraints.

(1) Is it possible that gate B has a setup-time violation and gate C has a setup-time violation? Explain why.

Yes. The violation path goes through both B and C.

(2) Is it possible that gate B has a setup-time violation and gate C has a hold-time violation? Explain why.

Yes. gate B has a large delay, so it has a setup-time violation, but gate C has a small delay, so it has a hold-time violation (the hold-time violation path comes from the lower path of gate C).

(3) Is it possible that gate B has a hold-time violation and gate C has a setup-time violation? Explain why.

Yes. Both gate B and gate C have short delays, but a gate connected to the output of gate C could have a long delay.

(4) Is it possible that gate B has a hold-time violation and gate C has a hold-time violation? Explain why.

Yes. Both gate B and gate C have very small delays, so a path going through gate B and gate C could violate a hold-time constraint.