EE434

ASIC and Digital Systems

Midterm Exam 1

Mar. 4, 2020. (2:10pm – 3pm)

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Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
Total	80	

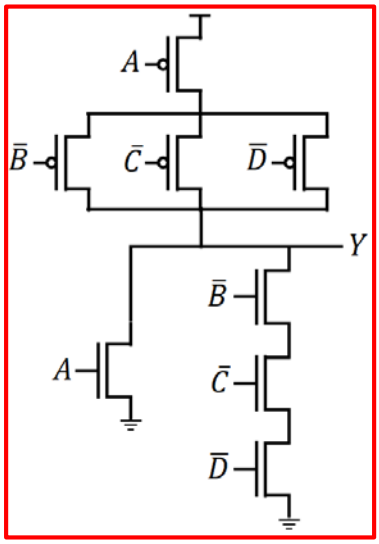
Problem #1 (Static CMOS gates, 10 points)

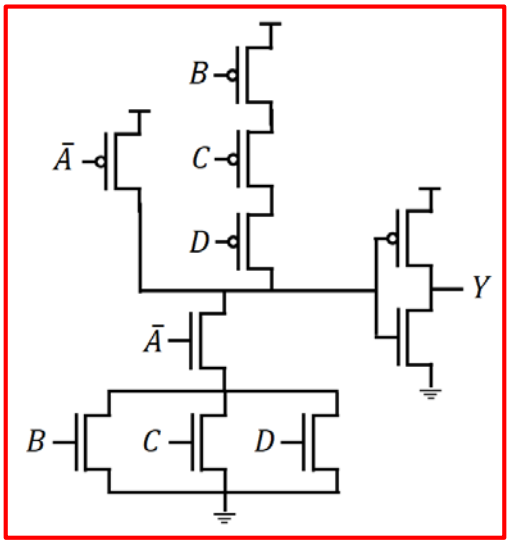
Design the following logic using the static CMOS design methodology. Try to minimize the # transistors. Available input: A, B, C, D.

$$Y = \overline{A + \bar{B} \cdot \bar{C} \cdot \bar{D}}$$

If we design it directly, we will need eight TRs + six TRs (for three inverters) = 14 TRs.

However, if we design $Y = \overline{\overline{A + \bar{B} \cdot \bar{C} \cdot \bar{D}}} = \overline{\bar{A} \cdot (B + C + D)}$, we will need eight TRs + four TRs (two for the inverter for $\bar{A}$ and two for the outer (last-level) inverter).





Left: 8 + 2 + 2 + 2 = 14 TRs (7 points)

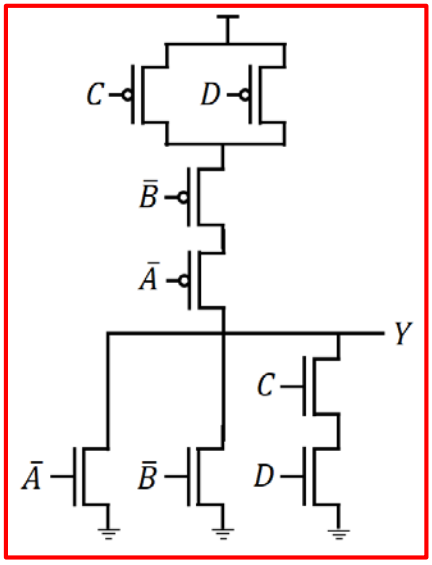
Right: 8 + 2 + 2 = 12 TRs (10 points)

Problem #2 (Static CMOS gates, 10 points)

Design the following logic using the static CMOS design methodology. Try to minimize the # transistors. Available input: A, B, C, D.

$$Y = A \cdot B \cdot (\bar{C} + \bar{D})$$

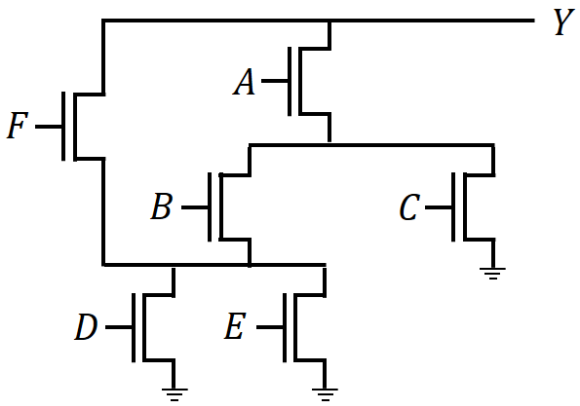
$$Y = \overline{\bar{A} + \bar{B} + C \cdot D}$$



8 + 4 = 12 TRs (10 points)

Problem #3 (Static CMOS gates, 10 points)

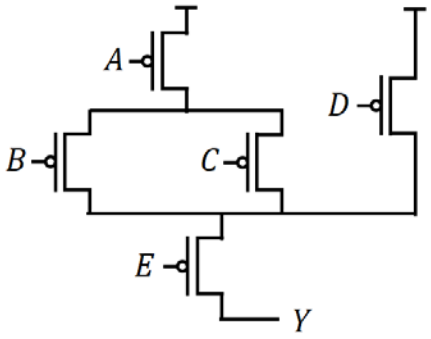
The following shows the NFET network of a static CMOS gate. Express the output Y as a Boolean function of the inputs (A~F). (You don't need to simplify the expression.)



$$Y = \overline{F(D + E + BC) + A(C + B(D + E))}$$

Problem #4 (Static CMOS gates, 10 points)

The following shows the PFET network of a static CMOS gate. Express the output Y as a Boolean function of the inputs (A~E). (You don't need to simplify the expression.)



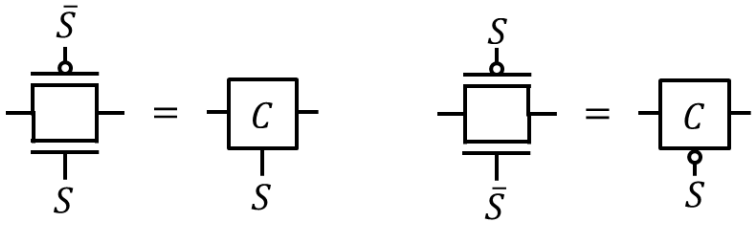
$$Y = (\bar{A} \cdot (\bar{B} + \bar{C}) + \bar{D}) \cdot \bar{E} = \overline{(A + BC) \cdot D + E}$$

Problem #5 (Transmission Gates, 10 points)

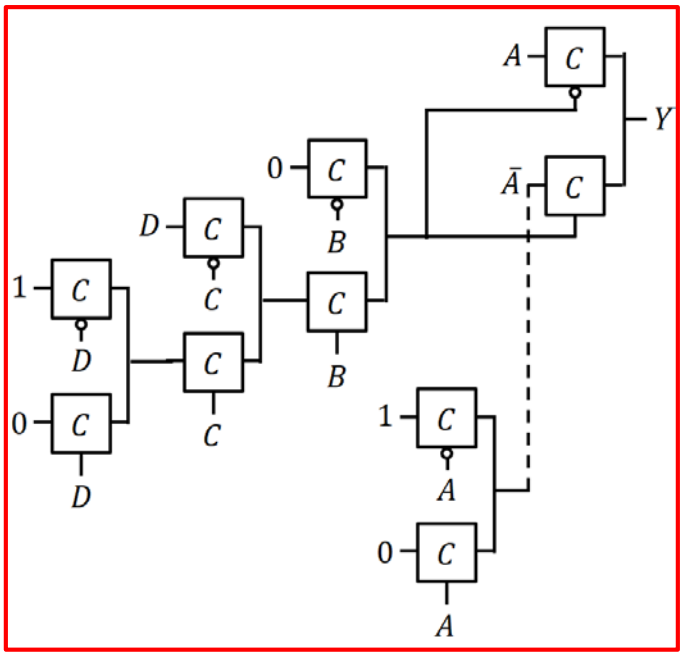
Design (draw a schematic) the following Boolean function using transmission gates only.

$$Y = A \oplus (B \cdot (C \oplus D))$$

Available inputs: $A, B, C, D, 0, 1$. Use the following symbols for the transmission gates.



(# TGs≤12: 10 points. 13≤# TGs≤15: 7 points. 16≤# TGs≤18: 5 points. # TGs>18: 3 points)



Problem #6 (Sequential Logic, 10 points)

The following truth table shows the function of a sequential logic. CK is the clock signal. A, B, D, E, and F are data or control (e.g., reset) signals. What does the gate do?? Explain the function in detail.

A	B	D	E	F	CK		Q^+
0	X	0	E	X	↓		E
0	X	1	X	F	↓		F
1	B	X	X	X	↓		B
X	X	X	X	X	↑		Q
X	X	X	X	X	0 or 1		Q

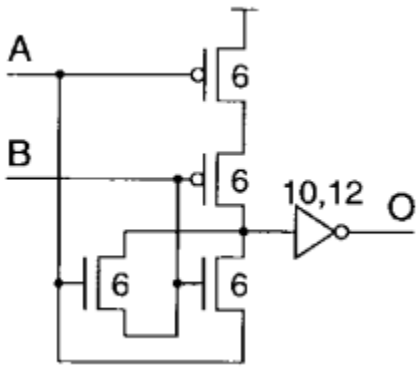
It is a negative-edge-triggered D-FF with the following features:

- A and D are used as input signal selectors as follows:
  - A=0, D=0: E is the data input.
  - A=0, D=1: F is the data input.
  - A=1: B is the data input.

Problem #7 (Analysis, 10 points)

What do the following circuits do? (You can ignore the numbers in the schematics.) For each schematic, you can draw a truth table or express the output as a function of the inputs.

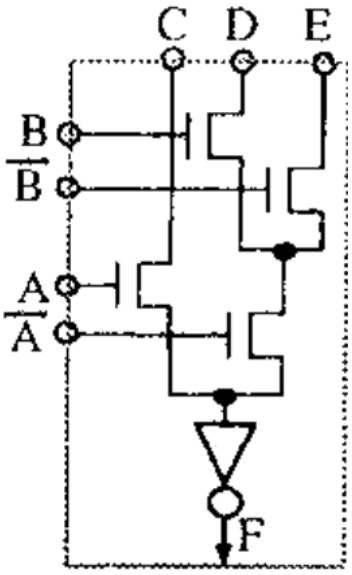
(a)



$O = A \cdot \bar{B} + \bar{A} \cdot B = A \oplus B$

(JSSC'97)

(b)

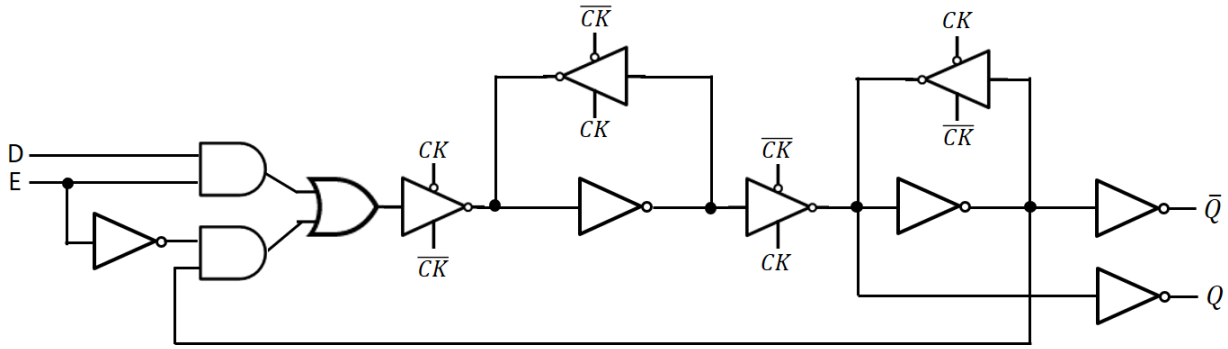


$F = A \cdot \bar{C} + \bar{A} \cdot (B \cdot \bar{D} + \bar{B} \cdot \bar{E})$

(JSSC'96)

Problem #8 (Sequential Logic, 10 points)

Explain the function of the following logic. CK: Clock. D, E: Data and/or control input.



If E=0, Q=hold regardless of the clock signal.

If E=1, it is a normal positive-edge-triggered D-F/F (in this case, D is the data input).